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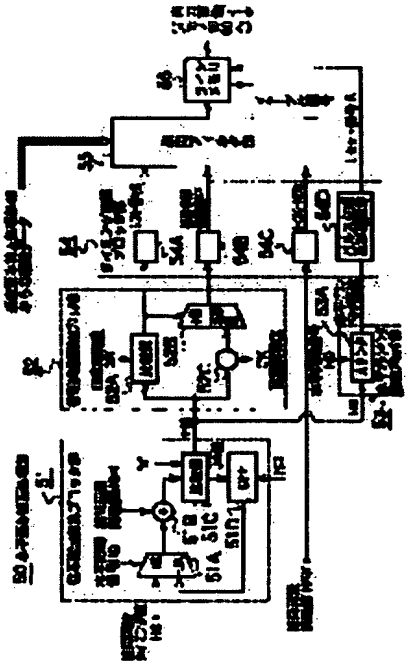
(54) TRAPEZOIDAL DISTORTION CORRECTING DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To electrically correct a trapezoidal distortion of a picture caused on a screen.

SOLUTION: When a horizontal trapezoidal distortion of a picture is corrected, this trapezoidal distortion correcting device is provided with a horizontal distortion correction processing part 50 having an interpolation filter part 55 for inputting an interval value GK between pixels adjacent in the horizontal direction in a liquid crystal panel 12, and horizontal distortion data correction data which is preset for each line according to a gate angle α (or β) to a projector 10 and a horizontal reduction rate or a horizontal enlargement ratio, and consists of an interpolation start timing value-HS for virtually starting interpolating pixels at the timing earlier than the top pixel of each line and an interpolated pixel interval value HGK of the adjacent interpolation pixel interval; calculating a target pixel to start interpolation in each line and an interpolation initial phase value XF for this target pixel to start interpolation from the interpolation start timing value and the interpolating pixel interval value; and performing pixel interpolation at each interpolation pixel interval value one after another from the position of the interpolation initial phase value for the target pixel to start interpolation in each line.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] A projector is installed in a slanting lower part or the slanting upper part to a screen. In the keystone distortion compensator which amends beforehand electrically the keystone distortion image produced on this screen when the image displayed on the display material in this projector is projected on said screen In case the horizontal keystone distortion of said image is amended, the horizontal adjacent pixel spacing value in said display material, According to the level contraction scale factor or level magnifying power to a gate angle and said image to said projector, it is beforehand set up for every Rhine. And the level distortion amendment data which consist of a interpolation initiation timing value for starting pixel interpolation virtually from the time of day when timing is earlier than the head pixel of each Rhine, and a interpolation pixel spacing value between adjacent interpolation pixels are inputted. The interpolation initial phase value from said interpolation initiation timing value and said interpolation pixel spacing value to the pixel for interpolation initiation of each Rhine and this pixel for interpolation initiation is computed. The keystone distortion compensator characterized by having the level distortion amendment processing section which has the interpolation filter section for performing pixel interpolation for said every interpolation pixel spacing value one after another for every Rhine from the location of said interpolation initial phase value to said pixel for interpolation initiation.
[Claim 2] In a keystone distortion compensator according to claim 1 said level distortion amendment processing section Round addition is carried out until this interpolation initiation timing value changes said interpolation pixel spacing value to a plus value to said interpolation initiation timing value which is a minus value incorporated to the timing of a Horizontal Synchronizing signal. When the plus value outputted from the scale-factor round addition block section which outputs a plus value, and said scale-factor round addition block section is smaller than said pixel spacing value The 1st shift signal which directs that the pixel for interpolation initiation is a head pixel is outputted. While outputting said plus value as said interpolation initial phase value to said head pixel as it is, and when said plus value is larger than said pixel spacing value The 2nd shift signal which directs that it is the following pixel whose pixel for interpolation initiation is a head pixel is outputted. And the interpolation initial phase detection block section which outputs the value which subtracted said pixel spacing value from said plus value as said interpolation initial phase value to said following pixel, Said 1st shift signal outputted from said interpolation initial phase detection block section or said 2nd shift signal, and said interpolation initial phase value, The keystone distortion compensator characterized by having the timing adjustment block section which carries out timing adjustment of said interpolation pixel spacing value, respectively, and is outputted to said interpolation filter section.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the keystone distortion compensator which amends beforehand the keystone distortion image produced on a screen electrically, when a projector is installed in a slanting lower part or the slanting upper part to a screen and the image from this projector is projected on a screen.
[0002]
[Description of the Prior Art] With arrival of digital multimedia age, television broadcasting is also expanded on a screen, CS digital broadcast to which digitization is accelerated and broadcast is already carried out, and images with which broadcast was put very much in practical use recently, such as BS digital broadcasting, can be projected, and the projector equipped with the electrochromatic display light valve which can also expand and project the computer image of a high definition on a screen attracts attention further.
[0003] Here, the projector of a front projection mold is installing the projector in a slanting lower part or the slanting upper part to a screen so that it may be put on the front side of a screen and existence of the projector itself may not usually become the hindrance of the appreciation to the image projected on the screen. A screen is installed in an parallel condition to the wall surface of the room, and, specifically, on the other hand, a projector is installed in the condition of having hung from above the floor level or head lining ahead [of a screen], in many cases. In addition, in the following explanation, it carries out projecting an image from an upper part side to a screen to calling it "projection from the upper part" like [at the time of installing conversely projecting an image from a lower part side to a screen in "projection from a lower part", a call, and the condition of having hung the projector from head lining, like / at the time of installing a projector above the floor level].
[0004] When an image is expanded and projected on a screen from a projector, drawing 1 Are drawing for explaining the keystone distortion image produced on a screen, and (a) shows the keystone distortion image by the projection from a lower part. Drawing and drawing 2 which showed the keystone distortion image according [(b)] to the projection from the upper part are drawing for explaining the amendment approach of the conventional keystone distortion image, and (a) and (b) are drawings having shown the case where the keystone distortion image shown in drawing 1 (a) and (b) was amended electrically, respectively.
[0005] As shown in drawing 1 (a), the projector 10 equipped with the electrochromatic display light valve is installed above the floor level here. And when the image displayed on the liquid crystal panel 12 used as display material is expanded on a screen 14 with a projector lens 13 and is projected with the light from the light source 11 in a projector 10 Since it instigates between 14h of normals of optical-axis 10k of a projector 10, and the center position of a screen 14 and angle alpha exists, without 14h of normals of optical-axis 10k of a projector 10 and the center position of a screen 14 being in agreement On a screen 14, the keystone distortion (keystone distortion) image DL with the die length of the surface longer than the die length of a base is generated.
[0006] On the other hand, as shown in drawing 1 (b), also when a projector 10 is installed in the

condition of having hung from head lining Since it instigates between 14h of normals of optical-axis 10k of a projector 10, and the center position of a screen 14 and angle beta exists, without 14h of normals of optical-axis 10k of a projector 10 and the center position of a screen 14 being in agreement On a screen 14, the keystone distortion (keystone distortion) image DU with the die length of the surface shorter than the die length of a base is generated.
[0007] Under the present circumstances, according to the gate angles alpha and beta which change with the installation conditions of a projector 10, the generating condition of the keystone distortion images DL and DU also changes.
[0008] When it instigates between 14h of normals of optical-axis 10k of a projector 10, and the center position of a screen 14 and angle alpha (or beta) exists, in order to make it the keystone distortion image DL (or DU) not arise on a screen 14 since it is such, the various proposals of the solution technique more nearly optical than before or the electric solution technique are made.
[0009] By preparing gate devices (for example, gate lens etc.) in the incident light study system of a projector 10, and adjusting the gate angle by the gate device concerned as a typical example of the optical solution technique Although the solution technique which amends the keystone distortion image DL (or DU) generated on a screen 14 exists, since a gate device etc. serves as cost quantity, the electric solution technique which carries out the following is adopted.
[0010] Here, as a typical example of the electric solution technique, only the part of the pixel which thinned out and thinned out the pixel as opposed to the subject-copy image before the projection displayed on the liquid crystal panel 12 in a projector 10 has added the blanking field to both ends, for example as indicated by JP,5-37880,A.
[0011] That is, after only the part of the pixel which thinned out the pixel for every Rhine, compressed and was thinned out so that it might become a trapezoid with the reverse upper and lower sides to the keystone distortion image DL which showed the image DLH for the keystone distortion amendment displayed on a liquid crystal panel 12 as shown at drawing 2 (a) in the projection from the lower part which installed the projector 10 above the floor level to drawing 1 (a) has added the blanking field to both ends, it has projected.
[0012] It has projected, after only the part of the pixel which thinned out the pixel for every Rhine, compressed and was thinned out so that it might become a trapezoid with the reverse upper and lower sides to the keystone distortion image DU which showed the image DUH for the keystone distortion amendment displayed on a liquid crystal panel 12 as shown at drawing 2 (b) in the projection from the upper part which hung the projector 10 from head lining on the other hand, and was installed to drawing 1 (b) has added the blanking field to both ends.
[0013]
[Problem(s) to be Solved by the Invention] By the way, the keystone distortion images DL and DU produced on a screen when a projector 10 is installed in a slanting lower part or the slanting upper part to a screen 14, as described above When amending electrically beforehand to the subject-copy image displayed on the liquid crystal panel 12 in a projector 10, the image DLH for keystone distortion amendment after carrying out keystone distortion amendment processing, or DUH Correlation is lost between Rhine where each other is perpendicularly adjoined since the number of Rhine is thinned out according to the perpendicular contraction scale factor to the perpendicular direction. And since correlation is lost also between the pixels which adjoin each other since it received horizontally and the horizontal number of pixels is thinned out for every Rhine It becomes the image with which the pixel shifted, where image quality is degraded remarkably, a keystone distortion image will be amended electrically, and the projection image of good image quality is not obtained on a screen 14.
[0014] Moreover, as the source projected using a projector etc., the high-definition digital color picture not only by the standard image by the NTSC signal (National Television System Committee) which is a video signal of the standard television system of our country but CS digital broadcast, BS digital broadcasting, etc., the computer image of the high definition dealt with with a personal computer, etc. are used in recent years.
[0015] Although the two-dimensional processing which performs processing of the vertical Rhine unit and processing of a horizontal pixel unit (dot unit) to coincidence is originally rational when

performing keystone distortion amendment processing electrically For example, the SXGA (Super eXtended Graphics Array) image which is one of the computer images dealt with with a personal computer Since 1024 lines is perpendicularly formed by 1280 pixels, and a rectangle-like effective image field is formed horizontally and the horizontal clock frequency of a SXGA signal becomes 100MHz or more and a high speed, large-scale, in order to have to process horizontal processing at a high speed per pixel (dot unit) especially, when performing two-dimensional processing for a perpendicular direction and a horizontal direction to coincidence at the time of keystone distortion amendment processing -- it is -- it is -- there are problems, such as needing a complicated hard configuration.

[0016] then -- between adjacent pixels with each Rhine horizontal [that the image for keystone distortion amendment after carrying out keystone distortion amendment processing has correlation between Rhine where each other is adjoined perpendicularly when performing keystone distortion amendment processing electrically] -- correlation -- it is -- amendment processing as horizontal moreover as vertical amendment processing -- another ******** -- a keystone distortion compensator with which a small-scale hard configuration can also perform keystone distortion amendment good is desired by things.

[0017]

[Means for Solving the Problem] This invention is made in view of the above-mentioned technical problem. The 1st invention A projector is installed in a slanting lower part or the slanting upper part to a screen. In the keystone distortion compensator which amends beforehand electrically the keystone distortion image produced on this screen when the image displayed on the display material in this projector is projected on said screen In case the horizontal keystone distortion of said image is amended, the horizontal adjacent pixel spacing value in said display material, According to the level contraction scale factor or level magnifying power to a gate angle and said image to said projector, it is beforehand set up for every Rhine. And the level distortion amendment data which consist of a interpolation initiation timing value for starting pixel interpolation virtually from the time of day when timing is earlier than the head pixel of each Rhine, and a interpolation pixel spacing value between adjacent interpolation pixels are inputted. The interpolation initial phase value from said interpolation initiation timing value and said interpolation pixel spacing value to the pixel for interpolation initiation of each Rhine and this pixel for interpolation initiation is computed. It is the keystone distortion compensator characterized by having the level distortion amendment processing section which has the interpolation filter section for performing pixel interpolation for said every interpolation pixel spacing value one after another for every Rhine from the location of said interpolation initial phase value to said pixel for interpolation initiation.

[0018] In the keystone distortion compensator of the 1st invention which described the 2nd invention above moreover, said level distortion amendment processing section Round addition is carried out until this interpolation initiation timing value changes said interpolation pixel spacing value to a plus value to said interpolation initiation timing value which is a minus value incorporated to the timing of a Horizontal Synchronizing signal. When the plus value outputted from the scale-factor round addition block section which outputs a plus value, and said scale-factor round addition block section is smaller than said pixel spacing value The 1st shift signal which directs that the pixel for interpolation initiation is a head pixel is outputted. While outputting said plus value as said interpolation initial phase value to said head pixel as it is, and when said plus value is larger than said pixel spacing value The 2nd shift signal which directs that it is the following pixel whose pixel for interpolation initiation is a head pixel is outputted. And the interpolation initial phase detection block section which outputs the value which subtracted said pixel spacing value from said plus value as said interpolation initial phase value to said following pixel, Said 1st shift signal outputted from said interpolation initial phase detection block section or said 2nd shift signal, and said interpolation initial phase value, It is the keystone distortion compensator characterized by having the timing adjustment block section which carries out timing adjustment of said interpolation pixel spacing value, respectively, and is outputted to said interpolation filter section.

[0019]

[Embodiment of the Invention] One example of the keystone distortion compensator concerning this invention is explained with reference to drawing 1 , drawing 3 , or drawing 11 below at a detail in order of <the whole keystone distortion compensator configuration and whole actuation>, the <perpendicular distortion amendment processing section>, and the <level distortion amendment processing section>.
[0020] The block diagram having shown the whole keystone distortion compensator configuration which <keystone distortion compensator whole configuration and whole actuation> drawing 3 requires for this invention, It is drawing shown typically [in order that drawing 4 may explain actuation by the whole keystone distortion compensator concerning this invention]. (a) shows the image array of a subject-copy image, and (b) shows the image array by perpendicular distortion amendment processing. Drawing having shown the image array of the image for keystone distortion amendment with which (c) is finally generated through perpendicular distortion amendment processing and level distortion amendment processing, Drawing 5 divides between Rhine of the perpendicular direction in a liquid crystal panel, and between the horizontal pixels of each Rhine with a predetermined number using the keystone distortion compensator concerning this invention at the time of perpendicular distortion amendment processing and level distortion amendment processing. It is drawing having shown the fundamental view at the time of acquiring a vertical interpolation phase value and a vertical horizontal interpolation phase value by this division.
[0021] As shown in drawing 3 , the keystone distortion compensator 20 concerning this invention is applied to the projector 10 (drawing 1) which used the electrochromatic display light valve etc., installs this projector 10 in a slanting lower part or the slanting upper part to a screen 14 (drawing 1), and when an image is expanded and projected on a screen 14 from a projector 10, it amends beforehand electrically the keystone distortion image produced on a screen 14. Under the present circumstances, the gate angle alpha shown in drawing 1 (a) or drawing 1 (b) to the screen 14 or the gate angle beta is given by installing in a slanting lower part or the slanting upper part, and the projector 10 is constituted so that the image for keystone distortion amendment may be obtained according to the perpendicular contraction scale factor and level contraction scale factor to this gate angle alpha or the gate angle beta, and an image.
[0022] In addition, it replaces with the perpendicular contraction scale factor and level contraction scale factor to an image, and it is also possible to obtain the image for keystone distortion amendment according to the perpendicular magnifying power and level magnifying power to an image, and it mentions later about this.
[0023] The keystone distortion compensator 20 concerning above-mentioned this invention While generating Vertical Synchronizing signal VD, Horizontal Synchronizing signal HD, etc. from input image data and controlling the whole equipment The perpendicular distortion amendment data for generating interpolation Rhine, thinning out the number of Rhine for the perpendicular direction of an image according to a perpendicular contraction scale factor, The control section 30 equipped with the memory table 31 which memorized the level distortion amendment data for carrying out pixel interpolation of the horizontal direction of an image, thinning out the number of pixels according to the level contraction scale factor for every Rhine according to the gate angle alpha to the screen 14 of a projector 10 (or beta), As opposed to the input image data displayed on the liquid crystal panel 12 in a projector 10 The perpendicular distortion amendment processing section 40 which performs vertical keystone distortion amendment processing per Rhine, The level distortion amendment processing section 50 which performs keystone distortion amendment processing that it is horizontal after performing vertical keystone distortion amendment processing, per pixel (dot unit) for every Rhine, The outline configuration is carried out from the memory section 60 of FIFO (FIFO) which outputs the image data which accumulated temporarily the image data after perpendicular distortion amendment processing and level distortion amendment processing, and was accumulated here to predetermined timing.
[0024] under the present circumstances, the perpendicular distortion amendment processing section 40 and the level distortion amendment processing section 50 -- another **** -- by carrying out independently each, in case it is dealt with with a personal computer, improvement in the speed of keystone distortion amendment processing and the miniaturization of a hard

scale are realized to the SXGA image which needs high-speed processing.
[0025] Perpendicular distortion amendment processing **** 40 carries out filtering processing of the Rhine spacing with pixel interpolation, thinning out the vertical number of Rhine according to a perpendicular contraction scale factor. Moreover, level distortion amendment processing **** 50 To between Rhine of the upper and lower sides which adjoin each other by carrying out filtering processing of the pixel spacing with pixel interpolation, thinning out the number of pixels according to a level contraction scale factor to the horizontal direction in each Rhine, functionality is given and functionality is given also between the horizontal adjacent pixels of each Rhine.
[0026] In addition, without restricting to this, after carrying out horizontal keystone distortion amendment processing previously, the sequence of the perpendicular distortion amendment processing section and the level distortion amendment processing section is replaced, and it is possible [in the keystone distortion compensator 20 by the above-mentioned configuration, after performing vertical keystone distortion amendment processing previously to input image data, horizontal keystone distortion amendment processing is performed, but] also in constituting so that vertical keystone distortion amendment processing may be carried out.
[0027] Next, in the projection from the lower part which installed the projector 10 in above the floor level [of a slanting lower part] as opposed to the screen 14, the concept of perpendicular distortion amendment processing and level distortion amendment processing is explained using drawing 4 (a) - (c).
[0028] As shown in drawing 4 (a), when it shall have N pixel horizontally and input image data is displayed on this liquid crystal panel 12 as it was, the subject-copy image by the pixel of a MxN individual of M lines (M pixels) is perpendicularly obtained in a liquid crystal panel 12.
[0029] On the other hand, as shown in drawing 4 (b), when the perpendicular distortion amendment processing section 40 in the keystone distortion compensator 20 performs vertical keystone distortion amendment processing per Rhine to input image data, Rhine of the perpendicular direction of a liquid crystal panel 12 serves as an image which the perpendicular contraction scale factor increased from the lower part to **** toward the upper part.
[0030] Furthermore, as shown in drawing 4 (c), after performing vertical keystone distortion amendment processing When the level distortion amendment processing section 50 performs horizontal keystone distortion amendment processing per pixel (dot unit) for every Rhine Each horizontal pixel of a liquid crystal panel 12 becomes large as a level contraction scale factor has a small lower part and goes up, and the image DHL for keystone distortion amendment in the condition of having reverse-amended beforehand the keystone distortion image produced on the screen is obtained.
[0031] Next, using the keystone distortion compensator 20, between Rhine of the perpendicular direction in a liquid crystal panel 12 and between the horizontal pixels of each Rhine are divided with a predetermined number at the time of perpendicular distortion amendment processing and level distortion amendment processing, and the fundamental view at the time of acquiring a vertical interpolation phase value and a vertical horizontal interpolation phase value by this division is previously described using drawing 5 .
[0032] As shown in drawing 5 , in the effective image field of the shape of a rectangle of a liquid crystal panel 12, corresponding to a SXGA image, 1024 lines (1024 pixels) are prepared perpendicularly, and the Rhine address uses 10 bits or more, and is given in each Rhine. On the other hand, 1280 pixels is prepared horizontally, and the pixel number is given using 11 bits or more to each pixel. In addition, pixel interpolation processing horizontal to bilateral symmetry is possible for a horizontal direction centering on the center section of each Rhine.
[0033] Moreover, both vertical Rhine spacing (= up-and-down pixel spacing) and horizontal adjacent pixel spacing of each Rhine are being set as the fixed spacing k and dividing into 32 steps by making the inside of the fixed spacing k into a predetermined number, and show this division value for k/32 by the number of steps using 5 bits as a unit value (= 1 step value) to a phase value.
[0034] And if the division value Y of the inside divided into 32 with the pixel data of each vertical Rhine as the starting point is perpendicularly set up for every Rhine as a vertical interpolation

phase value when carrying out pixel interpolation processing, the phase value Y over one Rhine and the remaining division value to next Rhine nearest to this one Rhine are (32−Y).
[0035] If similarly the division value X of the inside divided into 32 with each horizontal pixel of each Rhine as the starting point is set up for every pixel as a horizontal interpolation phase value when carrying out pixel interpolation processing horizontally, the phase value X over one pixel and the remaining division value to the following pixel nearest to this one pixel serve as (32−X).
[0036] In addition, what is necessary is just to set up the number of partitions N suitably according to the image quality precision of an image, although it checked that 32 division was good and set up in the example, if it corresponded to the SXGA image when dividing between Rhine and between pixels with a predetermined number.
[0037] In the keystone distortion compensator which <perpendicular distortion amendment processing section> drawing 6 requires for this invention, the block diagram and drawing 7 which showed the perpendicular distortion amendment processing section are drawing for explaining interpolation Rhine at the time of the perpendicular distortion amendment processing section performing perpendicular distortion amendment processing.
[0038] The perpendicular distortion amendment processing section 40 shown in drawing 6 is a thing based on Japanese Patent Application No. No. 359746 [11 to] previously proposed from these people. As opposed to the keystone distortion image which will be generated when the subject−copy image displayed on a liquid crystal panel 12 by the projector 10 (drawing 1) is expanded and projected on a screen 14 as it was In order to perform perpendicular distortion amendment processing for amending the keystone distortion about the perpendicular direction of an image especially to input image data, it has the interpolation filter section 41, the Rhine memory 42, the interpolation data change−over section 43, the line counter 44, and the comparator 45.
[0039] In the above−mentioned perpendicular distortion amendment processing section 40, input image data is sent to the interpolation filter section 41. The above−mentioned interpolation filter section 41 is equipped with the perpendicular filter for generating the data of interpolation Rhine based on the interpolation phase value Y to the image data of the perpendicular direction for every Rhine among input image data.
[0040] A control section 30 (drawing 3) here The gate angle alpha to the screen 14 of a projector 10 (or beta) As perpendicular distortion amendment data which interpolate Rhine of the perpendicular direction of an image according to the perpendicular contraction scale factor to an image The interpolation phase value Y of the perpendicularly which each Rhine address B for interpolation and each Rhine address B which are displayed using 11 bits, and a pair are made, and is displayed using 5 bits is read from the memory table 31 (drawing 3). While supplying each Rhine address B to a comparator 45, the vertical interpolation phase value Y is supplied to the interpolation filter section 41.
[0041] In addition, in this example, the perpendicular distortion amendment data memorized by the memory table 31 (drawing 3) are beforehand computed according to the gate angle alpha and perpendicular contraction scale factor at the time of projection from the lower part by the projector 10 [drawing 1 (a)].
[0042] Moreover, the control section 30 (drawing 3) supplies Vertical Synchronizing signal VD and Horizontal Synchronizing signal HD which generated Vertical Synchronizing signal VD and Horizontal Synchronizing signal HD, and were generated from input image data here to the line counter 44. And a line counter 44 counts the number of Rhine of input image data based on Vertical Synchronizing signal VD and Horizontal Synchronizing signal HD, and has sent the counted value to the comparator 45 as the address A of an input line.
[0043] The address A of an input line to which the above−mentioned comparator 45 was supplied from the line counter 44 (counted value) The sequential comparison of each Rhine address B for [which was supplied from the memory table 31 (drawing 3)] interpolation is carried out. When both address value is in agreement as a result of this comparison, the Rhine memory 42 and the interpolation data change−over section 43 are told about the enable signal which shows that the data of interpolation Rhine generated in the interpolation filter section 41 are effective (when it

is A=B).
[0044] On the other hand, sequential supply of the interpolation phase value Y of the perpendicularly each Rhine address B for interpolation and a pair are made is carried out from the memory table 31 (drawing 3) at the interpolation filter section 41, and the data of interpolation Rhine are generated based on the interpolation phase value Y between Rhine of the Rhine address B for interpolation, and Rhine of this near.
[0045] That is, using drawing 7 as an approach of generating the data of interpolation Rhine of the input image data in the interpolation filter section 41, the linear interpolation of two points is mentioned as an example, and is explained. Here, the linear interpolation of two points calculates the image data of Rhine of the adjacent upper and lower sides according to the ratio of a interpolation phase value, it is driving Rhine of the upper and lower sides which adjoin each other by this ratio, and interpolation Rhine is generated virtually.
[0046] As shown in drawing 7 , as for input image data, the sequential input of the image data [00] for every 1 level Rhine, [01], [02], and .. is carried out in the interpolation filter section 41 per Rhine at the Rhine addresses 00, 01, and 02 and the order of ....
[0047] And in the interpolation filter section 41, a interpolation operation is first performed as vertical two-point interpolation between the image data of the 00th line for interpolation [00], and the image data [01] of the 01st line. Under the present circumstances, since the division value Y which serves as vertical interpolation phase data to the image data [00] of the 00th line is beforehand set as 2 numbers of steps when between adjacent Rhine is divided into 32, for example, as drawing 5 explained, the remaining division value to next Rhine serves as the number-of-steps (32-Y) =30 number of steps. Therefore, in case the image data [00'] of interpolation Rhine is generated in the interpolation filter section 41, the operation of the following type is performed. [00'] =([00] x2+[01] x30) /32[0048] Next, between the 01st line and the 02nd line, since Rhine for interpolation is not set up, Rhine will be thinned out.
[0049] Next, since the division value Y which turns into a vertical interpolation phase value to the image data [02] of the 02nd line is beforehand set as 19 numbers of steps when performing a interpolation operation between the image data of the 02nd line for interpolation [02], and the image data [03] of the 03rd line, the remaining division value to next Rhine serves as the number-of-steps (32-Y) =13 number of steps. Therefore, in case the image data [01'] of interpolation Rhine is generated in the interpolation filter section 41, the operation of the following type is performed. [01'] =([02] x19+[03] x13) /32[0050] the following — the same — carrying out — Rhine — a number — perpendicular — contraction — a scale factor — having corresponded — interpolation — an object — each — Rhine — the address — B — following — — thinning out — having — while — Rhine — between — interpolating — things — interpolation — Rhine — image data — [— 00 — ' —] — [— 01 — ' —] — [— 02 — ' —] — [— 03 — ' —] .... order — henceforth — each — Rhine — ******** — interpolation — Rhine — generating — having .
[0051] And the image data of each interpolation Rhine outputted from the interpolation filter section 41 is temporarily stored in the Rhine memory 42 at each time when the enable signal from a comparator 45 was taken out, and the sequential output is carried out at the interpolation data change-over section 43.
[0052] Next, in the interpolation data change-over section 43, while outputting to the level distortion amendment processing section 50 which mentions later the image data of interpolation Rhine by which the sequential output was carried out from the Rhine memory 42 at each time when the enable signal from a comparator 45 was taken out, when an enable signal is not taken out, the constant data set as arbitration are outputted to the level distortion amendment processing section 50 side. Under the present circumstances, the constant data set as arbitration are data for masking Rhine other than effective Rhine of the image reduced by perpendicular distortion amendment processing. And the condition of drawing 4 (b) which explained previously the image data which performed perpendicular distortion amendment processing by the perpendicular distortion amendment processing section 40 is acquired.
[0053] Rhine of the Rhine address B for [corresponding to the perpendicular contraction scale factor to an image at the above-mentioned level distortion amendment processing section 50]

interpolation, By generating interpolation Rhine based on the interpolation phase value Y between Rhine of this near, and amending a vertical keystone distortion Since functionality can be given between interpolation Rhine where each other is adjoined perpendicularly, image quality degradation of the perpendicularly it generates in simple pixel infanticide at the time of perpendicular distortion amendment processing in which it explained in the conventional example can be pressed down.

[0054] In the keystone distortion compensator which <level distortion amendment processing section> drawing 8 requires for this invention Drawing for explaining the level direct distortion amendment data at the time of the block diagram and drawing 9 which showed the level distortion amendment processing section performing level direct distortion amendment processing by the level distortion amendment processing section, Drawing having shown the level direct distortion amendment data at the time of drawing 10 performing level direct distortion amendment processing by the level distortion amendment processing section on the chart and drawing 11 are drawings having shown the actuation which performs level direct distortion amendment processing by the level distortion amendment processing section.

[0055] As opposed to the keystone distortion image which will be generated when the level distortion amendment processing section 50 shown in drawing 8 expands the subject-copy image displayed on a liquid crystal panel 12 by the projector 10 (drawing 1) to a screen 14 as it was and projects it In order to perform level distortion amendment processing for amending the keystone distortion about the horizontal direction of an image especially to the image data from the perpendicular distortion amendment processing section 40 It has the scale-factor round addition block section 51, the interpolation initial phase detection block section 52, the level blanking detection block section 53, the timing adjustment block section 54, the interpolation filter section 55, and the Rhine memory 56.

[0056] In case level distortion amendment processing is performed in the level distortion amendment processing section 50, as shown in drawing 9 , here If the inside of the fixed spacing k between the pixels which adjoin each other all over each Rhine is divided into 32 steps as mentioned above, and it explains below by making 1/32xk into the number of unit steps (=1 number of steps) The pixel spacing value GK between adjacent pixels is memorized by the memory table 31 in a control section 30 (drawing 3), as each Rhine serves as 32 numbers of steps and this pixel spacing value GK was shown in drawing 10 .

[0057] Moreover, if pixel interpolation shall be virtually started from the time of day when timing is earlier than the 00th pixel which turns into a head pixel all over each Rhine as shown in drawing 9 This interpolation initiation timing value - HS The number of steps of interpolation initiation timing value-HS which is a minus value is beforehand set [with the 00th pixel as the starting point in each Rhine] up according to the gate angle alpha at the time of projection toward the minus (-) direction from the lower part by the projector 10 [drawing 1 (a)] for every Rhine. This interpolation initiation timing value - As HS was also shown in drawing 10 , the memory table 31 in a control section 30 (drawing 3) memorizes.

[0058] Moreover, the level contraction scale factor is beforehand set up for every Rhine, and this level contraction scale factor is permuted and displayed on the interpolation pixel spacing value HGK which carried out pixel interpolation horizontally all over each Rhine, as shown in drawing 9 . And as the number of steps of the interpolation pixel spacing value HGK of each Rhine is beforehand set up according to the gate angle alpha of a projector 10 and this interpolation pixel spacing value HGK was also shown in drawing 10 , the memory table 31 in a control section 30 (drawing 3) memorizes. Here, when the interpolation pixel spacing value HGK and the pixel spacing value HGK are in agreement, a level contraction scale factor is 1, many numbers of pixels more nearly horizontal as the interpolation pixel spacing value HGK becomes larger than the pixel spacing value HGK, a level contraction scale factor becomes large and a level contraction scale factor becomes larger will be thinned out, and pixel interpolation will be performed.

[0059] In case pixel interpolation is horizontally carried out all over each Rhine, moreover, among the horizontal interpolation phase values X over each pixel If the interpolation phase value over the first pixel for interpolation is called below the interpolation initial phase value XF, the first

pixel for interpolation in the 00th pixel which turns into a head pixel so that it may mention later Or it is either of the 01st pixels used as the next pixel of a head pixel, and the horizontal interpolation initial phase value XF at this time is computed by the scale-factor round addition block section 51 in the level distortion amendment processing section 50 shown in drawing 8 , and the interpolation initial phase detection block section 52.

[0060] Under the present circumstances, compute beforehand the interpolation phase value X over each pixel for interpolation all over each Rhine, and memory is made to memorize at the time of level distortion amendment processing. Since memory space will become immense if this approach is adopted although the same result is obtained also by the approach of performing pixel interpolation for every pixel based on the interpolation phase value X between the pixel for interpolation, and the pixel of this near, In this example, memory space is reduced by making the interpolation pixel spacing value HGK for carrying out pixel interpolation at the spacing same all over the same Rhine memorize with the interpolation initial phase value XF and this interpolation initial phase value XF of each Rhine as the starting point.

[0061] The scale-factor round addition block section 51 in return and the level distortion amendment processing section 50 is constituted by drawing 8 so that round addition may be performed by selector 51A, adder 51B, comparator 51C, and DFF(D flip-flop)51D.

[0062] And interpolation initiation timing value read from the memory table 31 in a control section 30 (drawing 3) to selector 51A of the scale-factor round addition block section 51 for every Rhine - HS is inputted as the number of steps of a minus value. The above-mentioned selector 51A is the inputted interpolation initiation timing value. - It is the round aggregate value which carries out the following to HS. - Chose either of the JA(s) to the timing of Horizontal Synchronizing signal HD, while chose, and it is a value. - HS or -JA is supplied to adder 51B.

[0063] Next, the interpolation pixel spacing value HGK read from the memory table 31 in a control section 30 (drawing 3) for every Rhine is inputted into adder 51B, and as this interpolation pixel spacing value HGK was mentioned above, according to the level contraction scale factor of each Rhine, the number of steps is set up beforehand. And in adder 51B, while chose by selector 51A, and it is a value. - The interpolation pixel spacing value HGK is added to HS or -JA. An addition result is inputted into comparator 51C. While comparator 51C compares an addition result here to zero value inputted beforehand, an addition result changes to the number of steps of a with a values of zero or more plus value and the number of steps of the plus value of cod roe is outputted to the interpolation initial phase detection block section 52 and the level blanking detection block section 53 Round aggregate value from which the addition result became a minus value smaller than zero value - Round addition is carried out until it will return an addition result to selector 51A through DFF(D flip-flop)51D and the addition result of adder 51B will change to a plus value, if it is the number of steps of JA. Under the present circumstances, in order to show whether an addition result changes the interpolation pixel spacing value HGK to a plus value by adding how many times, counting can be carried out as the count N of a round showed drawing 10 .

[0064] That is, selector 51A is a interpolation initiation timing value. - When HS is inputted, it is this interpolation initiation timing value. - HS is supplied to adder 51B. It is a interpolation initiation timing value at adder 51B. - HS and the interpolation pixel spacing value HGK are added, and this addition result is the round aggregate value of a minus value. - If it is JA This round aggregate value - JA goes round to selector 51A and selector 51A is a round aggregate value at the following timing. - JA is chosen, and round addition will be repeated until the addition result in adder 51B changes to the number of steps of a plus value by comparator 51C. Therefore, the number of steps of the plus value outputted from a comparator 51 is the interpolation initiation timing value set up in the minus direction with the 00th pixel of each Rhine as the starting point. - It is the direction where HS is reverse, and the origin of the 00th pixel will be carried out and the value of the number of steps of a plus direction will be acquired.

[0065] Next, the interpolation initial phase detection block section 52 in the level distortion amendment processing section 50 consists of comparator 52A, selector 52B, and subtractor 52C.

[0066] Here, the number of steps of the plus value outputted from comparator 51C of the scale-

factor round addition block section 51 is inputted into comparator 52A in the interpolation initial phase detection block section 52, and a selector 52B list at subtractor 52C. Furthermore, 32 numbers of steps are beforehand inputted into comparator 52A in the interpolation initial phase detection block section 52, and subtractor 52C as a pixel spacing value GK read from the memory table 31 in a control section 30 (drawing 3).

[0067] Here in comparator 52A of the interpolation initial phase detection block section 52 It asks whether the number of steps of the plus value outputted from comparator 51C of the scale-factor round addition block section 51 is larger than the pixel spacing value GK=32 number of steps to the pixel spacing value GK=32 number of steps inputted beforehand. When the number of steps of this plus value is smaller than the pixel spacing value GK, the 1st shift signal S= 0 is outputted. In being large, while outputting the 2nd shift signal S= 1 and controlling selector 52B by this 1st shift signal S= 0 or the 2nd shift signal S= 1 Furthermore, timing adjustment was carried out through timing regulator 54A in the timing adjustment block section 54, and the 1st shift signal S= 0 or the 2nd shift signal S= 1 is inputted into the interpolation filter section 55.

[0068] Under the present circumstances, the 1st shift signal S= 0 or the 2nd shift signal S= 1 inputted into the interpolation filter section 55 When it is functioning as a control signal for setting up the pixel for interpolation initiation and the 1st shift signal S= 0 is inputted, as for the pixel for interpolation initiation, each Rhine serves as the 00th pixel. On the other hand, when the 2nd shift signal S= 1 is inputted, as for the pixel for interpolation initiation, each Rhine serves as the 01st pixel.

[0069] Moreover, when the 1st shift signal S= 0 is supplied to selector 52B Selector 52B carries out timing adjustment of the number of steps of a plus value smaller than the pixel spacing value GK=32 number of steps outputted from comparator 51C of the scale-factor round addition block section 51 through timing regulator 54B in the timing adjustment block section 54 from selector 52B as it is. The number of steps of a plus value smaller than the pixel spacing value GK=32 number of steps is inputted into the interpolation filter section 55 as a horizontal interpolation initial phase value XF. The horizontal interpolation initial phase value XF acquired here corresponds to the 00th pixel, as described above as a pixel for interpolation initiation.

[0070] On the other hand, when the 2nd shift signal S= 1 is supplied to selector 52B Selector 52B subtracts the pixel spacing value GK=32 number of steps from the number of steps of a larger plus value than the pixel spacing value GK=32 number of steps outputted from comparator 51C of the scale-factor round addition block section 51 inputted into subtractor 52C. Timing adjustment of the number of steps of the subtraction result of having become small is carried out through timing regulator 54B in the timing adjustment block section 54 from the pixel spacing value GK=32 number of steps. The number of steps of a result which subtracted is inputted into the interpolation filter section 55 as a horizontal interpolation initial phase value XF, and the horizontal interpolation initial phase value XF acquired here corresponds to the 01st pixel, as described above as a pixel for interpolation initiation.

[0071] Moreover, the interpolation pixel spacing value HGK read from the memory table 31 in a control section 30 (drawing 3) for every Rhine carried out timing adjustment through timing regulator 54C in the timing adjustment block section 54, and is inputted into the interpolation filter section 55 as new interpolation pixel spacing value HGK-NEW after timing adjustment. Under the present circumstances, new interpolation pixel spacing value HGK-NEW after timing adjustment is the same number of steps as the number of steps of the interpolation pixel spacing value HGK memorized by the memory table 31, and timing adjustment is only made.

[0072] Moreover, the number of steps of zero or more (plus value) values outputted from comparator 51C in the scale-factor round addition block section 51 is inputted into counter 53A in the level blanking detection block section 53 as a level blanking width-of-face generation control signal HB, and Horizontal Synchronizing signal HD is inputted into this counter 53A. And counter 53A is reset to the timing of Horizontal Synchronizing signal HD, is stopping a count with the level blanking width-of-face generation control signal HB, computes the number of steps of zero or more (plus value) values outputted for every Rhine from comparator 51C in the scale-factor round addition block section 51 as a level bulan GINGU width-of-face value, and supplies

it to the pulse generation in the timing adjustment block section 54, and delay section 54D. Then, in the pulse generation in the timing adjustment block section 54, and delay section 54D, reset-signal R to the Rhine memory 56 is generated based on a level bulan GINGU width-of-face value.

[0073] From the above, it is based on new interpolation pixel spacing value HGK-NEW after the 1st shift signal S= 0 or the 2nd shift signal S= 1, the horizontal interpolation initial phase value XF, and timing adjustment in the interpolation filter section 55. Level distortion amendment processing is performed by carrying out pixel interpolation for every Rhine to the image data outputted from the perpendicular distortion amendment processing section 40. When an enable signal is outputted, it accumulates in the Rhine memory 56 temporarily for every Rhine, and after this, from the Rhine memory 56, sequential are recording is carried out and the image data of each Rhine is hereafter explained to the memory section (FIFO) 60 shown in drawing 3 concretely.
[0074] As shown in drawing 9 and drawing 10 , according to the gate angle alpha at the time of the projection from the lower part of a projector 10 { drawing 1 (a)}, and the level contraction scale factor to an image, the pixel spacing value GK, interpolation initiation timing value-HS, and the interpolation pixel spacing value HGK are beforehand memorized as level distortion amendment data by the memory table 31 in a control section 30 (drawing 3).
[0075] First, since it is beforehand set as the adjacent pixel spacing value GK=32 number of steps, the interpolation initiation timing value-HS=-84 number of steps, and the interpolation pixel spacing value HGK=56 number of steps in the 00th line In the scale-factor round addition block section 51 shown in drawing 8 , by two round addition The output value from comparator 51C in this scale-factor round addition block section 51 will change to the number of steps of plus, namely, the number of steps of -HS+HGK+HGK=-84+56+56=28 is obtained in the scale-factor round addition block section 51.
[0076] Then, at comparator 52A in the interpolation initial-valve-position detection block section 52 shown in drawing 8 , in the scale-factor round addition block section 51, since the ********** 28 number of steps is smaller than the pixel spacing value GK in the scale-factor round addition block section 51 to the ********** 28 number of steps as compared with the pixel spacing value GK=32 number of steps, the 1st shift signal S= 0 is supplied to selector 52B and the interpolation filter section 55 from comparator 52A. Here, selector 52B is outputted to the interpolation filter section 55 as it is in the scale-factor round addition block section 51 with the control signal of the 1st shift signal S= 0 by making the ********** 28 number of steps into the interpolation initial phase value XF=28 number of steps.
[0077] As shown in drawing 9 and drawing 11 , in the interpolation filter section 55, with therefore, the inputted 1st shift signal S= 0 to the 00th line Interpolation is started from the location where the pixel for interpolation initiation is the 00th pixel of the 00th line, and becomes the number of steps of interpolation initial phase value XF=28 with this 00th pixel as the starting point. Level distortion amendment is performed to the 00th line by carrying out pixel interpolation along with 00 lines every interpolation pixel spacing value HGK=56 number of steps from this interpolation initial valve position.
[0078] Next, since it is beforehand set as the adjacent pixel spacing value GK=32 number of steps, the interpolation initiation timing value-HS=-77 number of steps, and the interpolation pixel spacing value HGK=54 number of steps in the 01st line Like the 00th above-mentioned line, in the scale-factor round addition block section 51 by two round addition The output value from comparator 51C in this scale-factor round addition block section 51 will change to the number of steps of plus, namely, the number of steps of -HS+HGK+HGK=-77+54+54=31 is obtained in the scale-factor round addition block section 51.
[0079] Then, in the interpolation initial-valve-position detection block section 52, since the ********** 31 number of steps is smaller than the pixel spacing value GK=32 number of steps in the scale-factor round addition block section 51, the 1st shift signal S= 0 and the interpolation initial phase value XF=31 number of steps are outputted to the interpolation filter section 55 like the 00th above-mentioned line.
[0080] As shown in drawing 9 , in the interpolation filter section 55, with therefore, the inputted

1st shift signal S= 0 to the 01st line Interpolation is started from the location where the pixel for interpolation initiation is the 00th pixel of the 01st line, and becomes the interpolation initial phase value XF=31 number of steps with this 00th pixel as the starting point. Level distortion amendment is performed to the 01st line by carrying out pixel interpolation along with 01 lines every interpolation pixel spacing value HGK=54 number of steps from this interpolation initial valve position.

[0081] Next, since it is beforehand set as the adjacent pixel spacing value GK=32 number of steps, the interpolation initiation timing value-HS=-70 number of steps, and the interpolation pixel spacing value HGK=52 number of steps in the 02nd line Like the 00th above-mentioned line and the 01st line, in the scale-factor round addition block section 51 by two round addition The output value from this scale-factor round addition block section 51 will change to the number of steps of plus, namely, the number of steps of -HS+HGK+HGK=-70+52+52=34 is obtained in the scale-factor round addition block section 51.

[0082] Then, at comparator 52A in the interpolation initial-valve-position detection block section 52, in the scale-factor round addition block section 51, since the ********** 34 number of steps is larger than the pixel spacing value GK in the scale-factor round addition block section 51 to the ********** 34 number of steps as compared with the pixel spacing value GK=32 number of steps, the 2nd shift signal S= 1 is supplied to selector 52B and the interpolation filter section 55 from comparator 52A. Here, selector 52B is outputted to the interpolation filter section 55 by making into the interpolation initial phase value XF=2 number of steps the number of steps of a result which subtracted [with the control signal of the 2nd shift signal S= 1] the pixel spacing value GK=32 number of steps to the ********** 34 number of steps in the scale-factor round addition block section 51 by subtractor 52C, i.e., the number of steps of 34-32=2.

[0083] As shown in drawing 9 and drawing 11 , in the interpolation filter section 55, with therefore, the inputted 2nd shift signal S= 1 to the 02nd line Interpolation is started from the location where the pixel for interpolation initiation is the 01st pixel of the 02nd line, and becomes the interpolation initial phase value XF=2 number of steps with this 01st pixel as the starting point. Level distortion amendment is performed to the 02nd line by carrying out pixel interpolation along with 02 lines every interpolation pixel spacing value HGK=52 number of steps from this interpolation initial valve position.

[0084] As described above, hereafter in the case of the 1st shift signal S= 0 Each Rhine starts pixel interpolation from the interpolation initial phase value XF over the 00th pixel. Level distortion amendment processing is performed for every interpolation pixel spacing value HGK of each Rhine. On the other hand, in the case of the 2nd CIF signal S= 1. Each Rhine started pixel interpolation from the interpolation initial phase value XF over the 01st pixel, carried out pixel interpolation for every interpolation pixel spacing value HGK one after another from this starting position, and has performed level distortion amendment processing.

[0085] Under the present circumstances, as shown in drawing 9 , along with the arrow head H which showed the interpolation starting position in each Rhine with the two-dot chain line, the 00th pixel turns into a pixel for interpolation initiation by the 00th line and the 01st line. The 01st pixel turns into a pixel for interpolation initiation to 02nd line - the 05th line, to 06th line - the 12th line, the 00th pixel turns into a pixel for interpolation initiation, and the image DHL for keystone distortion amendment as shown in drawing 4 (c) on the whole is memorized by the memory section 60 (drawing 3).

[0086] In addition, if level distortion amendment processing of each Rhine is performed as mentioned above to the center section of each Rhine and it carries out to bilateral symmetry centering on this center section, the image DHL for keystone distortion amendment as shown in drawing 4 (c) will be obtained.

[0087] Interpolation initiation timing value which starts interpolation virtually for every Rhine in the above-mentioned level distortion amendment processing section 50 - HS is changed. Change the interpolation initial phase value XF for every Rhine, and for every Rhine further by and the thing for which the interpolation pixel spacing value HGK equivalent to the level contraction scale factor to an image is changed, pixel interpolation is performed for every Rhine, and a

horizontal keystone distortion is amended Since functionality can be given between the interpolation pixels which each horizontal Rhine adjoins, horizontal image quality degradation generated in simple pixel infanticide at the time of level distortion amendment processing in which it explained in the conventional example can be pressed down.
[0088] Although the perpendicular distortion amendment processing section 40 and the level distortion amendment processing section 50 mentioned the linear interpolation of two points as an example and explained generation of vertical interpolation Rhine, and horizontal pixel interpolation of each Rhine with the keystone distortion compensator concerning this invention explained in full detail above, it is applicable also to the four-point interpolation processing which increased the number of Rhine, and the number of pixels at the time of interpolation.
[0089] Furthermore, although it explained that keystone distortion amendment processing was performed according to the gate angle alpha (or beta), the perpendicular direction, the perpendicular contraction scale factor that receives horizontally, and level contraction scale factor to a screen 14 of a projector 10 when obtaining the image DHL for keystone distortion amendment It is also possible to perform keystone distortion amendment processing to the above and reverse according to the gate angle alpha (or beta), the perpendicular direction, the perpendicular magnifying power that receives horizontally, and level magnifying power to a screen 14 of a projector 10. Thus, what is necessary is just to perform level distortion amendment processing in the direction which accumulates input image data in memory in advance, and performs perpendicular distortion amendment processing in the direction which the number of Rhine increases from this memory according to perpendicular magnifying power, and the horizontal number of pixels increases according to level magnifying power, in performing keystone distortion amendment processing, expanding an image to input image data.
[0090]
[Effect of the Invention] According to the keystone distortion amendment circuit concerning this invention explained in full detail above, especially in the level distortion amendment processing section The interpolation initiation timing value which starts interpolation virtually for every Rhine is changed. Change a interpolation initial phase value for every Rhine, and for every Rhine further by and the thing for which a interpolation pixel spacing value equivalent to the level contraction scale factor to an image or perpendicular magnifying power is changed, pixel interpolation is performed for every Rhine, and a horizontal keystone distortion is amended Since functionality can be given between the interpolation pixels which each horizontal Rhine adjoins, horizontal image quality degradation generated in simple pixel infanticide at the time of level distortion amendment processing in which it explained in the conventional example can be pressed down. Moreover, in the level distortion amendment processing section, since what is necessary is just to store a pixel spacing value, and the interpolation initiation timing value of each Rhine and a interpolation pixel spacing value in a memory table, storage capacity of a memory table can be made small.

[Translation done.]

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the keystone distortion compensator which amends beforehand the keystone distortion image produced on a screen electrically, when a projector is installed in a slanting lower part or the slanting upper part to a screen and the image from this projector is projected on a screen.

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PRIOR ART

[Description of the Prior Art] With arrival of digital multimedia age, television broadcasting is also expanded on a screen, CS digital broadcast to which digitization is accelerated and broadcast is already carried out, and images with which broadcast was put very much in practical use recently, such as BS digital broadcasting, can be projected, and the projector equipped with the electrochromatic display light valve which can also expand and project the computer image of a high definition on a screen attracts attention further.
[0003] Here, the projector of a front projection mold is installing the projector in a slanting lower part or the slanting upper part to a screen so that it may be put on the front side of a screen and existence of the projector itself may not usually become the hindrance of the appreciation to the image projected on the screen. A screen is installed in an parallel condition to the wall surface of the room, and, specifically, on the other hand, a projector is installed in the condition of having hung from above the floor level or head lining ahead [of a screen], in many cases. In addition, in the following explanation, it carries out projecting an image from an upper part side to a screen to calling it "projection from the upper part" like [at the time of installing conversely projecting an image from a lower part side to a screen in "projection from a lower part", a call, and the condition of having hung the projector from head lining, like / at the time of installing a projector above the floor level].
[0004] When an image is expanded and projected on a screen from a projector, drawing 1 Are drawing for explaining the keystone distortion image produced on a screen, and (a) shows the keystone distortion image by the projection from a lower part. Drawing and drawing 2 which showed the keystone distortion image according [(b)] to the projection from the upper part are drawing for explaining the amendment approach of the conventional keystone distortion image, and (a) and (b) are drawings having shown the case where the keystone distortion image shown in drawing 1 (a) and (b) was amended electrically, respectively.
[0005] As shown in drawing 1 (a), the projector 10 equipped with the electrochromatic display light valve is installed above the floor level here. And when the image displayed on the liquid crystal panel 12 used as display material is expanded on a screen 14 with a projector lens 13 and is projected with the light from the light source 11 in a projector 10 Since it instigates between 14h of normals of optical-axis 10k of a projector 10, and the center position of a screen 14 and angle alpha exists, without 14h of normals of optical-axis 10k of a projector 10 and the center position of a screen 14 being in agreement On a screen 14, the keystone distortion (keystone distortion) image DL with the die length of the surface longer than the die length of a base is generated.
[0006] On the other hand, as shown in drawing 1 (b), also when a projector 10 is installed in the condition of having hung from head lining Since it instigates between 14h of normals of optical-axis 10k of a projector 10, and the center position of a screen 14 and angle beta exists, without 14h of normals of optical-axis 10k of a projector 10 and the center position of a screen 14 being in agreement On a screen 14, the keystone distortion (keystone distortion) image DU with the die length of the surface shorter than the die length of a base is generated.
[0007] Under the present circumstances, according to the gate angles alpha and beta which change with the installation conditions of a projector 10, the generating condition of the

keystone distortion images DL and DU also changes.
[0008] When it instigates between 14h of normals of optical-axis 10k of a projector 10, and the center position of a screen 14 and angle alpha (or beta) exists, in order to make it the keystone distortion image DL (or DU) not arise on a screen 14 since it is such, the various proposals of the solution technique more nearly optical than before or the electric solution technique are made.
[0009] By preparing gate devices (for example, gate lens etc.) in the incident light study system of a projector 10, and adjusting the gate angle by the gate device concerned as a typical example of the optical solution technique Although the solution technique which amends the keystone distortion image DL (or DU) generated on a screen 14 exists, since a gate device etc. serves as cost quantity, the electric solution technique which carries out the following is adopted.
[0010] Here, as a typical example of the electric solution technique, only the part of the pixel which thinned out and thinned out the pixel as opposed to the subject-copy image before the projection displayed on the liquid crystal panel 12 in a projector 10 has added the blanking field to both ends, for example as indicated by JP,5-37880,A.
[0011] That is, after only the part of the pixel which thinned out the pixel for every Rhine, compressed and was thinned out so that it might become a trapezoid with the reverse upper and lower sides to the keystone distortion image DL which showed the image DLH for the keystone distortion amendment displayed on a liquid crystal panel 12 as shown at drawing 2 (a) in the projection from the lower part which installed the projector 10 above the floor level to drawing 1 (a) has added the blanking field to both ends, it has projected.
[0012] It has projected, after only the part of the pixel which thinned out the pixel for every Rhine, compressed and was thinned out so that it might become a trapezoid with the reverse upper and lower sides to the keystone distortion image DU which showed the image DUH for the keystone distortion amendment displayed on a liquid crystal panel 12 as shown at drawing 2 (b) in the projection from the upper part which hung the projector 10 from head lining on the other hand, and was installed to drawing 1 (b) has added the blanking field to both ends.

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EFFECT OF THE INVENTION

[Effect of the Invention] According to the keystone distortion amendment circuit concerning this invention explained in full detail above, at the level distortion amendment processing section, it is especially, The interpolation initiation timing value which starts interpolation virtually for every Rhine is changed. Change a interpolation initial phase value for every Rhine, and for every Rhine further by and the thing for which a interpolation pixel spacing value equivalent to the level contraction scale factor to an image or perpendicular magnifying power is changed, pixel interpolation is performed for every Rhine, and a horizontal keystone distortion is amended Since functionality can be given between the interpolation pixels which each horizontal Rhine adjoins, horizontal image quality degradation generated in simple pixel infanticide at the time of level distortion amendment processing in which it explained in the conventional example can be pressed down. Moreover, in the level distortion amendment processing section, since what is necessary is just to store a pixel spacing value, and the interpolation initiation timing value of each Rhine and a interpolation pixel spacing value in a memory table, storage capacity of a memory table can be made small.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] By the way, the keystone distortion images DL and DU produced on a screen when a projector 10 is installed in a slanting lower part or the slanting upper part to a screen 14, as described above When amending electrically beforehand to the subject-copy image displayed on the liquid crystal panel 12 in a projector 10, the image DLH for keystone distortion amendment after carrying out keystone distortion amendment processing, or DUH Correlation is lost between Rhine where each other is perpendicularly adjoined since the number of Rhine is thinned out according to the perpendicular contraction scale factor to the perpendicular direction. And since correlation is lost also between the pixels which adjoin each other since it received horizontally and the horizontal number of pixels is thinned out for every Rhine It becomes the image with which the pixel shifted, where image quality is degraded remarkably, a keystone distortion image will be amended electrically, and the projection image of good image quality is not obtained on a screen 14.
[0014] Moreover, as the source projected using a projector etc., the high-definition digital color picture not only by the standard image by the NTSC signal (National Television System Committee) which is a video signal of the standard television system of our country but CS digital broadcast, BS digital broadcasting, etc., the computer image of the high definition dealt with with a personal computer, etc. are used in recent years.
[0015] Although the two-dimensional processing which performs processing of the vertical Rhine unit and processing of a horizontal pixel unit (dot unit) to coincidence is originally rational when performing keystone distortion amendment processing electrically For example, the SXGA (Super eXtended Graphics Array) image which is one of the computer images dealt with with a personal computer Since 1024 lines is perpendicularly formed by 1280 pixels, and a rectangle-like effective image field is formed horizontally and the horizontal clock frequency of a SXGA signal becomes 100MHz or more and a high speed, large-scale, in order to have to process horizontal processing at a high speed per pixel (dot unit) especially, when performing two-dimensional processing for a perpendicular direction and a horizontal direction to coincidence at the time of keystone distortion amendment processing — it is -- it is — there are problems, such as needing a complicated hard configuration.
[0016] then — between adjacent pixels with each Rhine horizontal [that the image for keystone distortion amendment after carrying out keystone distortion amendment processing has correlation between Rhine where each other is adjoined perpendicularly when performing keystone distortion amendment processing electrically] — correlation — it is — amendment processing as horizontal moreover as vertical amendment processing — another ******** — a keystone distortion compensator with which a small-scale hard configuration can also perform keystone distortion amendment good is desired by things.

[Translation done.]

MEANS

[Means for Solving the Problem] This invention is made in view of the above-mentioned technical problem. The 1st invention A projector is installed in a slanting lower part or the slanting upper part to a screen. In the keystone distortion compensator which amends beforehand electrically the keystone distortion image produced on this screen when the image displayed on the display material in this projector is projected on said screen In case the horizontal keystone distortion of said image is amended, the horizontal adjacent pixel spacing value in said display material, According to the level contraction scale factor or level magnifying power to a gate angle and said image to said projector, it is beforehand set up for every Rhine. And the level distortion amendment data which consist of a interpolation initiation timing value for starting pixel interpolation virtually from the time of day when timing is earlier than the head pixel of each Rhine, and a interpolation pixel spacing value between adjacent interpolation pixels are inputted. The interpolation initial phase value from said interpolation initiation timing value and said interpolation pixel spacing value to the pixel for interpolation initiation of each Rhine and this pixel for interpolation initiation is computed. It is the keystone distortion compensator characterized by having the level distortion amendment processing section which has the interpolation filter section for performing pixel interpolation for said every interpolation pixel spacing value one after another for every Rhine from the location of said interpolation initial phase value to said pixel for interpolation initiation.
[0018] In the keystone distortion compensator of the 1st invention which described the 2nd invention above moreover, said level distortion amendment processing section Round addition is carried out until this interpolation initiation timing value changes said interpolation pixel spacing value to a plus value to said interpolation initiation timing value which is a minus value incorporated to the timing of a Horizontal Synchronizing signal. When the plus value outputted from the scale-factor round addition block section which outputs a plus value, and said scale-factor round addition block section is smaller than said pixel spacing value The 1st shift signal which directs that the pixel for interpolation initiation is a head pixel is outputted. While outputting said plus value as said interpolation initial phase value to said head pixel as it is, and when said plus value is larger than said pixel spacing value The 2nd shift signal which directs that it is the following pixel whose pixel for interpolation initiation is a head pixel is outputted. And the interpolation initial phase detection block section which outputs the value which subtracted said pixel spacing value from said plus value as said interpolation initial phase value to said following pixel, Said 1st shift signal outputted from said interpolation initial phase detection block section or said 2nd shift signal, and said interpolation initial phase value, It is the keystone distortion compensator characterized by having the timing adjustment block section which carries out timing adjustment of said interpolation pixel spacing value, respectively, and is outputted to said interpolation filter section.
[0019]
[Embodiment of the Invention] One example of the keystone distortion compensator concerning this invention is explained with reference to drawing 1 , drawing 3 , or drawing 11 below at a detail in order of <the whole keystone distortion compensator configuration and whole actuation>, the <perpendicular distortion amendment processing section>, and the <level

distortion amendment processing section>.
[0020] The block diagram having shown the whole keystone distortion compensator configuration which <keystone distortion compensator whole configuration and whole actuation> drawing 3 requires for this invention, It is drawing shown typically [in order that drawing 4 may explain actuation by the whole keystone distortion compensator concerning this invention]. (a) shows the image array of a subject-copy image, and (b) shows the image array by perpendicular distortion amendment processing. Drawing having shown the image array of the image for keystone distortion amendment with which (c) is finally generated through perpendicular distortion amendment processing and level distortion amendment processing, Drawing 5 divides between Rhine of the perpendicular direction in a liquid crystal panel, and between the horizontal pixels of each Rhine with a predetermined number using the keystone distortion compensator concerning this invention at the time of perpendicular distortion amendment processing and level distortion amendment processing. It is drawing having shown the fundamental view at the time of acquiring a vertical interpolation phase value and a vertical horizontal interpolation phase value by this division.
[0021] As shown in drawing 3 , the keystone distortion compensator 20 concerning this invention is applied to the projector 10 (drawing 1) which used the electrochromatic display light valve etc., installs this projector 10 in a slanting lower part or the slanting upper part to a screen 14 (drawing 1), and when an image is expanded and projected on a screen 14 from a projector 10, it amends beforehand electrically the keystone distortion image produced on a screen 14. Under the present circumstances, the gate angle alpha shown in drawing 1 (a) or drawing 1 (b) to the screen 14 or the gate angle beta is given by installing in a slanting lower part or the slanting upper part, and the projector 10 is constituted so that the image for keystone distortion amendment may be obtained according to the perpendicular contraction scale factor and level contraction scale factor to this gate angle alpha or the gate angle beta, and an image.
[0022] In addition, it replaces with the perpendicular contraction scale factor and level contraction scale factor to an image, and it is also possible to obtain the image for keystone distortion amendment according to the perpendicular magnifying power and level magnifying power to an image, and it mentions later about this.
[0023] The keystone distortion compensator 20 concerning above-mentioned this invention While generating Vertical Synchronizing signal VD, Horizontal Synchronizing signal HD, etc. from input image data and controlling the whole equipment The perpendicular distortion amendment data for generating interpolation Rhine, thinning out the number of Rhine for the perpendicular direction of an image according to a perpendicular contraction scale factor, The control section 30 equipped with the memory table 31 which memorized the level distortion amendment data for carrying out pixel interpolation of the horizontal direction of an image, thinning out the number of pixels according to the level contraction scale factor for every Rhine according to the gate angle alpha to the screen 14 of a projector 10 (or beta), As opposed to the input image data displayed on the liquid crystal panel 12 in a projector 10 The perpendicular distortion amendment processing section 40 which performs vertical keystone distortion amendment processing per Rhine, The level distortion amendment processing section 50 which performs keystone distortion amendment processing that it is horizontal after performing vertical keystone distortion amendment processing, per pixel (dot unit) for every Rhine, The outline configuration is carried out from the memory section 60 of FIFO (FIFO) which outputs the image data which accumulated temporarily the image data after perpendicular distortion amendment processing and level distortion amendment processing, and was accumulated here to predetermined timing.
[0024] under the present circumstances, the perpendicular distortion amendment processing section 40 and the level distortion amendment processing section 50 — another **** — by carrying out independently each, in case it is dealt with with a personal computer, improvement in the speed of keystone distortion amendment processing and the miniaturization of a hard scale are realized to the SXGA image which needs high-speed processing.
[0025] Perpendicular distortion amendment processing **** 40 carries out filtering processing of the Rhine spacing with pixel interpolation, thinning out the vertical number of Rhine according to a perpendicular contraction scale factor. Moreover, level distortion amendment processing ****

50 To between Rhine of the upper and lower sides which adjoin each other by carrying out filtering processing of the pixel spacing with pixel interpolation, thinning out the number of pixels according to a level contraction scale factor to the horizontal direction in each Rhine, functionality is given and functionality is given also between the horizontal adjacent pixels of each Rhine.

[0026] In addition, without restricting to this, after carrying out horizontal keystone distortion amendment processing previously, the sequence of the perpendicular distortion amendment processing section and the level distortion amendment processing section is replaced, and it is possible [in the keystone distortion compensator 20 by the above-mentioned configuration, after performing vertical keystone distortion amendment processing previously to input image data, horizontal keystone distortion amendment processing is performed, but] also in constituting so that vertical keystone distortion amendment processing may be carried out.

[0027] Next, in the projection from the lower part which installed the projector 10 in above the floor level [of a slanting lower part] as opposed to the screen 14, the concept of perpendicular distortion amendment processing and level distortion amendment processing is explained using drawing 4 (a) - (c).

[0028] As shown in drawing 4 (a), when it shall have N pixel horizontally and input image data is displayed on this liquid crystal panel 12 as it was, the subject-copy image by the pixel of a MxN individual of M lines (M pixels) is perpendicularly obtained in a liquid crystal panel 12.

[0029] On the other hand, as shown in drawing 4 (b), when the perpendicular distortion amendment processing section 40 in the keystone distortion compensator 20 performs vertical keystone distortion amendment processing per Rhine to input image data, Rhine of the perpendicular direction of a liquid crystal panel 12 serves as an image which the perpendicular contraction scale factor increased from the lower part to **** toward the upper part.

[0030] Furthermore, as shown in drawing 4 (c), after performing vertical keystone distortion amendment processing When the level distortion amendment processing section 50 performs horizontal keystone distortion amendment processing per pixel (dot unit) for every Rhine Each horizontal pixel of a liquid crystal panel 12 becomes large as a level contraction scale factor has a small lower part and goes up, and the image DHL for keystone distortion amendment in the condition of having reverse-amended beforehand the keystone distortion image produced on the screen is obtained.

[0031] Next, using the keystone distortion compensator 20, between Rhine of the perpendicular direction in a liquid crystal panel 12 and between the horizontal pixels of each Rhine are divided with a predetermined number at the time of perpendicular distortion amendment processing and level distortion amendment processing, and the fundamental view at the time of acquiring a vertical interpolation phase value and a vertical horizontal interpolation phase value by this division is previously described using drawing 5 .

[0032] As shown in drawing 5 , in the effective image field of the shape of a rectangle of a liquid crystal panel 12, corresponding to a SXGA image, 1024 lines (1024 pixels) are prepared perpendicularly, and the Rhine address uses 10 bits or more, and is given in each Rhine. On the other hand, 1280 pixels is prepared horizontally, and the pixel number is given using 11 bits or more to each pixel. In addition, pixel interpolation processing horizontal to bilateral symmetry is possible for a horizontal direction centering on the center section of each Rhine.

[0033] Moreover, both vertical Rhine spacing (= up-and-down pixel spacing) and horizontal adjacent pixel spacing of each Rhine are being set as the fixed spacing k and dividing into 32 steps by making the inside of the fixed spacing k into a predetermined number, and show this division value for k/32 by the number of steps using 5 bits as a unit value (= 1 step value) to a phase value.

[0034] And if the division value Y of the inside divided into 32 with the pixel data of each vertical Rhine as the starting point is perpendicularly set up for every Rhine as a vertical interpolation phase value when carrying out pixel interpolation processing, the phase value Y over one Rhine and the remaining division value to next Rhine nearest to this one Rhine are (32-Y).

[0035] If similarly the division value X of the inside divided into 32 with each horizontal pixel of each Rhine as the starting point is set up for every pixel as a horizontal interpolation phase

value when carrying out pixel interpolation processing horizontally, the phase value X over one pixel and the remaining division value to the following pixel nearest to this one pixel serve as (32−X).

[0036] In addition, what is necessary is just to set up the number of partitions N suitably according to the image quality precision of an image, although it checked that 32 division was good and set up in the example, if it corresponded to the SXGA image when dividing between Rhine and between pixels with a predetermined number.

[0037] In the keystone distortion compensator which <perpendicular distortion amendment processing section> drawing 6 requires for this invention, the block diagram and drawing 7 which showed the perpendicular distortion amendment processing section are drawing for explaining interpolation Rhine at the time of the perpendicular distortion amendment processing section performing perpendicular distortion amendment processing.

[0038] The perpendicular distortion amendment processing section 40 shown in drawing 6 is a thing based on Japanese Patent Application No. No. 359746 [11 to] previously proposed from these people. As opposed to the keystone distortion image which will be generated when the subject−copy image displayed on a liquid crystal panel 12 by the projector 10 (drawing 1) is expanded and projected on a screen 14 as it was In order to perform perpendicular distortion amendment processing for amending the keystone distortion about the perpendicular direction of an image especially to input image data, it has the interpolation filter section 41, the Rhine memory 42, the interpolation data change−over section 43, the line counter 44, and the comparator 45.

[0039] In the above−mentioned perpendicular distortion amendment processing section 40, input image data is sent to the interpolation filter section 41. The above−mentioned interpolation filter section 41 is equipped with the perpendicular filter for generating the data of interpolation Rhine based on the interpolation phase value Y to the image data of the perpendicular direction for every Rhine among input image data.

[0040] A control section 30 (drawing 3) here The gate angle alpha to the screen 14 of a projector 10 (or beta) As perpendicular distortion amendment data which interpolate Rhine of the perpendicular direction of an image according to the perpendicular contraction scale factor to an image The interpolation phase value Y of the perpendicularly which each Rhine address B for interpolation and each Rhine address B which are displayed using 11 bits, and a pair are made, and is displayed using 5 bits is read from the memory table 31 (drawing 3). While supplying each Rhine address B to a comparator 45, the vertical interpolation phase value Y is supplied to the interpolation filter section 41.

[0041] In addition, in this example, the perpendicular distortion amendment data memorized by the memory table 31 (drawing 3) are beforehand computed according to the gate angle alpha and perpendicular contraction scale factor at the time of projection from the lower part by the projector 10 [drawing 1 (a)].

[0042] Moreover, the control section 30 (drawing 3) supplies Vertical Synchronizing signal VD and Horizontal Synchronizing signal HD which generated Vertical Synchronizing signal VD and Horizontal Synchronizing signal HD, and were generated from input image data here to the line counter 44. And a line counter 44 counts the number of Rhine of input image data based on Vertical Synchronizing signal VD and Horizontal Synchronizing signal HD, and has sent the counted value to the comparator 45 as the address A of an input line.

[0043] The address A of an input line to which the above−mentioned comparator 45 was supplied from the line counter 44 (counted value) The sequential comparison of each Rhine address B for [which was supplied from the memory table 31 (drawing 3)] interpolation is carried out. When both address value is in agreement as a result of this comparison, the Rhine memory 42 and the interpolation data change−over section 43 are told about the enable signal which shows that the data of interpolation Rhine generated in the interpolation filter section 41 are effective (when it is A=B).

[0044] On the other hand, sequential supply of the interpolation phase value Y of the perpendicularly each Rhine address B for interpolation and a pair are made is carried out from the memory table 31 (drawing 3) at the interpolation filter section 41, and the data of

interpolation Rhine are generated based on the interpolation phase value Y between Rhine of the Rhine address B for interpolation, and Rhine of this near.
[0045] That is, using drawing 7 as an approach of generating the data of interpolation Rhine of the input image data in the interpolation filter section 41, the linear interpolation of two points is mentioned as an example, and is explained. Here, the linear interpolation of two points calculates the image data of Rhine of the adjacent upper and lower sides according to the ratio of a interpolation phase value, it is driving Rhine of the upper and lower sides which adjoin each other by this ratio, and interpolation Rhine is generated virtually.
[0046] As shown in drawing 7 , as for input image data, the sequential input of the image data [00] for every 1 level Rhine, [01], [02], and .. is carried out in the interpolation filter section 41 per Rhine at the Rhine addresses 00, 01, and 02 and the order of ....
[0047] And in the interpolation filter section 41, a interpolation operation is first performed as vertical two-point interpolation between the image data of the 00th line for interpolation [00], and the image data [01] of the 01st line. Under the present circumstances, since the division value Y which serves as vertical interpolation phase data to the image data [00] of the 00th line is beforehand set as 2 numbers of steps when between adjacent Rhine is divided into 32, for example, as drawing 5 explained, the remaining division value to next Rhine serves as the number-of-steps (32-Y) =30 number of steps. Therefore, in case the image data [00'] of interpolation Rhine is generated in the interpolation filter section 41, the operation of the following type is performed. [00'] =([00] x2+[01] x30) /32[0048] Next, between the 01st line and the 02nd line, since Rhine for interpolation is not set up, Rhine will be thinned out.
[0049] Next, since the division value Y which turns into a vertical interpolation phase value to the image data [02] of the 02nd line is beforehand set as 19 numbers of steps when performing a interpolation operation between the image data of the 02nd line for interpolation [02], and the image data [03] of the 03rd line, the remaining division value to next Rhine serves as the number-of-steps (32-Y) =13 number of steps. Therefore, in case the image data [01'] of interpolation Rhine is generated in the interpolation filter section 41, the operation of the following type is performed. [01'] =([02] x19+[03] x13) /32[0050] the following — the same — carrying out — Rhine — a number — perpendicular — contraction — a scale factor — having corresponded — interpolation — an object — each — Rhine — the address — B — following — thinning out — having — while — Rhine — between — interpolating — things — interpolation — Rhine — image data — [— 00 — ' —] — [— 01 — ' —] — [— 02 — ' —] — [— 03 — ' —] .... order — henceforth — each — Rhine — ******** — interpolation — Rhine — generating — having .
[0051] And the image data of each interpolation Rhine outputted from the interpolation filter section 41 is temporarily stored in the Rhine memory 42 at each time when the enable signal from a comparator 45 was taken out, and the sequential output is carried out at the interpolation data change-over section 43.
[0052] Next, in the interpolation data change-over section 43, while outputting to the level distortion amendment processing section 50 which mentions later the image data of interpolation Rhine by which the sequential output was carried out from the Rhine memory 42 at each time when the enable signal from a comparator 45 was taken out, when an enable signal is not taken out, the constant data set as arbitration are outputted to the level distortion amendment processing section 50 side. Under the present circumstances, the constant data set as arbitration are data for masking Rhine other than effective Rhine of the image reduced by perpendicular distortion amendment processing. And the condition of drawing 4 (b) which explained previously the image data which performed perpendicular distortion amendment processing by the perpendicular distortion amendment processing section 40 is acquired.
[0053] Rhine of the Rhine address B for [corresponding to the perpendicular contraction scale factor to an image at the above-mentioned level distortion amendment processing section 50] interpolation, By generating interpolation Rhine based on the interpolation phase value Y between Rhine of this near, and amending a vertical keystone distortion Since functionality can be given between interpolation Rhine where each other is adjoined perpendicularly, image quality degradation of the perpendicularly it generates in simple pixel infanticide at the time of

perpendicular distortion amendment processing in which it explained in the conventional example can be pressed down.
[0054] In the keystone distortion compensator which <level distortion amendment processing section> drawing 8 requires for this invention Drawing for explaining the level direct distortion amendment data at the time of the block diagram and drawing 9 which showed the level distortion amendment processing section performing level direct distortion amendment processing by the level distortion amendment processing section, Drawing having shown the level direct distortion amendment data at the time of drawing 10 performing level direct distortion amendment processing by the level distortion amendment processing section on the chart and drawing 11 are drawings having shown the actuation which performs level direct distortion amendment processing by the level distortion amendment processing section.
[0055] As opposed to the keystone distortion image which will be generated when the level distortion amendment processing section 50 shown in drawing 8 expands the subject-copy image displayed on a liquid crystal panel 12 by the projector 10 (drawing 1) to a screen 14 as it was and projects it In order to perform level distortion amendment processing for amending the keystone distortion about the horizontal direction of an image especially to the image data from the perpendicular distortion amendment processing section 40 It has the scale-factor round addition block section 51, the interpolation initial phase detection block section 52, the level blanking detection block section 53, the timing adjustment block section 54, the interpolation filter section 55, and the Rhine memory 56.
[0056] In case level distortion amendment processing is performed in the level distortion amendment processing section 50, as shown in drawing 9 , here If the inside of the fixed spacing k between the pixels which adjoin each other all over each Rhine is divided into 32 steps as mentioned above, and it explains below by making 1/32xk into the number of unit steps (=1 number of steps) The pixel spacing value GK between adjacent pixels is memorized by the memory table 31 in a control section 30 (drawing 3), as each Rhine serves as 32 numbers of steps and this pixel spacing value GK was shown in drawing 10 .
[0057] Moreover, if pixel interpolation shall be virtually started from the time of day when timing is earlier than the 00th pixel which turns into a head pixel all over each Rhine as shown in drawing 9 This interpolation initiation timing value - HS The number of steps of interpolation initiation timing value-HS which is a minus value is beforehand set [with the 00th pixel as the starting point in each Rhine] up according to the gate angle alpha at the time of projection toward the minus (-) direction from the lower part by the projector 10 { drawing 1 (a)} for every Rhine. This interpolation initiation timing value - As HS was also shown in drawing 10 , the memory table 31 in a control section 30 (drawing 3) memorizes.
[0058] Moreover, the level contraction scale factor is beforehand set up for every Rhine, and this level contraction scale factor is permuted and displayed on the interpolation pixel spacing value HGK which carried out pixel interpolation horizontally all over each Rhine, as shown in drawing 9 . And as the number of steps of the interpolation pixel spacing value HGK of each Rhine is beforehand set up according to the gate angle alpha of a projector 10 and this interpolation pixel spacing value HGK was also shown in drawing 10 , the memory table 31 in a control section 30 (drawing 3) memorizes. Here, when the interpolation pixel spacing value HGK and the pixel spacing value HGK are in agreement, a level contraction scale factor is 1, many numbers of pixels more nearly horizontal as the interpolation pixel spacing value HGK becomes larger than the pixel spacing value HGK, a level contraction scale factor becomes large and a level contraction scale factor becomes larger will be thinned out, and pixel interpolation will be performed.
[0059] In case pixel interpolation is horizontally carried out all over each Rhine, moreover, among the horizontal interpolation phase values X over each pixel If the interpolation phase value over the first pixel for interpolation is called below the interpolation initial phase value XF, the first pixel for interpolation in the 00th pixel which turns into a head pixel so that it may mention later Or it is either of the 01st pixels used as the next pixel of a head pixel, and the horizontal interpolation initial phase value XF at this time is computed by the scale-factor round addition block section 51 in the level distortion amendment processing section 50 shown in drawing 8 ,

and the interpolation initial phase detection block section 52.
[0060] Under the present circumstances, compute beforehand the interpolation phase value X over each pixel for interpolation all over each Rhine, and memory is made to memorize at the time of level distortion amendment processing. Since memory space will become immense if this approach is adopted although the same result is obtained also by the approach of performing pixel interpolation for every pixel based on the interpolation phase value X between the pixel for interpolation, and the pixel of this near, In this example, memory space is reduced by making the interpolation pixel spacing value HGK for carrying out pixel interpolation at the spacing same all over the same Rhine memorize with the interpolation initial phase value XF and this interpolation initial phase value XF of each Rhine as the starting point.
[0061] The scale-factor round addition block section 51 in return and the level distortion amendment processing section 50 is constituted by drawing 8 so that round addition may be performed by selector 51A, adder 51B, comparator 51C, and DFF(D flip-flop)51D.
[0062] And interpolation initiation timing value read from the memory table 31 in a control section 30 (drawing 3) to selector 51A of the scale-factor round addition block section 51 for every Rhine - HS is inputted as the number of steps of a minus value. The above-mentioned selector 51A is the inputted interpolation initiation timing value. - It is the round aggregate value which carries out the following to HS. - Chose either of the JA(s) to the timing of Horizontal Synchronizing signal HD, while chose, and it is a value. - HS or -JA is supplied to adder 51B.
[0063] Next, the interpolation pixel spacing value HGK read from the memory table 31 in a control section 30 (drawing 3) for every Rhine is inputted into adder 51B, and as this interpolation pixel spacing value HGK was mentioned above, according to the level contraction scale factor of each Rhine, the number of steps is set up beforehand. And in adder 51B, while chose by selector 51A, and it is a value. - The interpolation pixel spacing value HGK is added to HS or -JA. An addition result is inputted into comparator 51C. While comparator 51C compares an addition result here to zero value inputted beforehand, an addition result changes to the number of steps of a with a values of zero or more plus value and the number of steps of the plus value of cod roe is outputted to the interpolation initial phase detection block section 52 and the level blanking detection block section 53 Round aggregate value from which the addition result became a minus value smaller than zero value - Round addition is carried out until it will return an addition result to selector 51A through DFF(D flip-flop)51D and the addition result of adder 51B will change to a plus value, if it is the number of steps of JA. Under the present circumstances, in order to show whether an addition result changes the interpolation pixel spacing value HGK to a plus value by adding how many times, counting can be carried out as the count N of a round showed drawing 10 .
[0064] That is, selector 51A is a interpolation initiation timing value. - When HS is inputted, it is this interpolation initiation timing value. - HS is supplied to adder 51B. It is a interpolation initiation timing value at adder 51B. - HS and the interpolation pixel spacing value HGK are added, and this addition result is the round aggregate value of a minus value. - If it is JA This round aggregate value - JA goes round to selector 51A and selector 51A is a round aggregate value at the following timing. - JA is chosen, and round addition will be repeated until the addition result in adder 51B changes to the number of steps of a plus value by comparator 51C. Therefore, the number of steps of the plus value outputted from a comparator 51 is the interpolation initiation timing value set up in the minus direction with the 00th pixel of each Rhine as the starting point. - It is the direction where HS is reverse, and the origin of the 00th pixel will be carried out and the value of the number of steps of a plus direction will be acquired.
[0065] Next, the interpolation initial phase detection block section 52 in the level distortion amendment processing section 50 consists of comparator 52A, selector 52B, and subtractor 52C.
[0066] Here, the number of steps of the plus value outputted from comparator 51C of the scale-factor round addition block section 51 is inputted into comparator 52A in the interpolation initial phase detection block section 52, and a selector 52B list at subtractor 52C. Furthermore, 32 numbers of steps are beforehand inputted into comparator 52A in the interpolation initial phase detection block section 52, and subtractor 52C as a pixel spacing value GK read from the

memory table 31 in a control section 30 (drawing 3).
[0067] Here in comparator 52A of the interpolation initial phase detection block section 52 It asks whether the number of steps of the plus value outputted from comparator 51C of the scale-factor round addition block section 51 is larger than the pixel spacing value GK=32 number of steps to the pixel spacing value GK=32 number of steps inputted beforehand. When the number of steps of this plus value is smaller than the pixel spacing value GK, the 1st shift signal S= 0 is outputted. In being large, while outputting the 2nd shift signal S= 1 and controlling selector 52B by this 1st shift signal S= 0 or the 2nd shift signal S= 1 Furthermore, timing adjustment was carried out through timing regulator 54A in the timing adjustment block section 54, and the 1st shift signal S= 0 or the 2nd shift signal S= 1 is inputted into the interpolation filter section 55.
[0068] Under the present circumstances, the 1st shift signal S= 0 or the 2nd shift signal S= 1 inputted into the interpolation filter section 55 When it is functioning as a control signal for setting up the pixel for interpolation initiation and the 1st shift signal S= 0 is inputted, as for the pixel for interpolation initiation, each Rhine serves as the 00th pixel. On the other hand, when the 2nd shift signal S= 1 is inputted, as for the pixel for interpolation initiation, each Rhine serves as the 01st pixel.
[0069] Moreover, when the 1st shift signal S= 0 is supplied to selector 52B Selector 52B carries out timing adjustment of the number of steps of a plus value smaller than the pixel spacing value GK=32 number of steps outputted from comparator 51C of the scale-factor round addition block section 51 through timing regulator 54B in the timing adjustment block section 54 from selector 52B as it is. The number of steps of a plus value smaller than the pixel spacing value GK=32 number of steps is inputted into the interpolation filter section 55 as a horizontal interpolation initial phase value XF. The horizontal interpolation initial phase value XF acquired here corresponds to the 00th pixel, as described above as a pixel for interpolation initiation.
[0070] On the other hand, when the 2nd shift signal S= 1 is supplied to selector 52B Selector 52B subtracts the pixel spacing value GK=32 number of steps from the number of steps of a larger plus value than the pixel spacing value GK=32 number of steps outputted from comparator 51C of the scale-factor round addition block section 51 inputted into subtractor 52C. Timing adjustment of the number of steps of the subtraction result of having become small is carried out through timing regulator 54B in the timing adjustment block section 54 from the pixel spacing value GK=32 number of steps. The number of steps of a result which subtracted is inputted into the interpolation filter section 55 as a horizontal interpolation initial phase value XF, and the horizontal interpolation initial phase value XF acquired here corresponds to the 01st pixel, as described above as a pixel for interpolation initiation.
[0071] Moreover, the interpolation pixel spacing value HGK read from the memory table 31 in a control section 30 (drawing 3) for every Rhine carried out timing adjustment through timing regulator 54C in the timing adjustment block section 54, and is inputted into the interpolation filter section 55 as new interpolation pixel spacing value HGK-NEW after timing adjustment. Under the present circumstances, new interpolation pixel spacing value HGK-NEW after timing adjustment is the same number of steps as the number of steps of the interpolation pixel spacing value HGK memorized by the memory table 31, and timing adjustment is only made.
[0072] Moreover, the number of steps of zero or more (plus value) values outputted from comparator 51C in the scale-factor round addition block section 51 is inputted into counter 53A in the level blanking detection block section 53 as a level blanking width-of-face generation control signal HB, and Horizontal Synchronizing signal HD is inputted into this counter 53A. And counter 53A is reset to the timing of Horizontal Synchronizing signal HD, is stopping a count with the level blanking width-of-face generation control signal HB, computes the number of steps of zero or more (plus value) values outputted for every Rhine from comparator 51C in the scale-factor round addition block section 51 as a level bulan GINGU width-of-face value, and supplies it to the pulse generation in the timing adjustment block section 54, and delay section 54D. Then, in the pulse generation in the timing adjustment block section 54, and delay section 54D, reset-signal R to the Rhine memory 56 is generated based on a level bulan GINGU width-of-face value.

[0073] From the above, it is based on new interpolation pixel spacing value HGK-NEW after the 1st shift signal S= 0 or the 2nd shift signal S= 1, the horizontal interpolation initial phase value XF, and timing adjustment in the interpolation filter section 55. Level distortion amendment processing is performed by carrying out pixel interpolation for every Rhine to the image data outputted from the perpendicular distortion amendment processing section 40. When an enable signal is outputted, it accumulates in the Rhine memory 56 temporarily for every Rhine, and after this, from the Rhine memory 56, sequential are recording is carried out and the image data of each Rhine is hereafter explained to the memory section (FIFO) 60 shown in drawing 3 concretely.

[0074] As shown in drawing 9 and drawing 10 , according to the gate angle alpha at the time of the projection from the lower part of a projector 10 { drawing 1 (a)}, and the level contraction scale factor to an image, the pixel spacing value GK, interpolation initiation timing value-HS, and the interpolation pixel spacing value HGK are beforehand memorized as level distortion amendment data by the memory table 31 in a control section 30 (drawing 3).

[0075] First, since it is beforehand set as the adjacent pixel spacing value GK=32 number of steps, the interpolation initiation timing value-HS=-84 number of steps, and the interpolation pixel spacing value HGK=56 number of steps in the 00th line In the scale-factor round addition block section 51 shown in drawing 8 , by two round addition The output value from comparator 51C in this scale-factor round addition block section 51 will change to the number of steps of plus, namely, the number of steps of -HS+HGK+HGK=-84+56+56=28 is obtained in the scale-factor round addition block section 51.

[0076] Then, at comparator 52A in the interpolation initial-valve-position detection block section 52 shown in drawing 8 , in the scale-factor round addition block section 51, since the ********** 28 number of steps is smaller than the pixel spacing value GK in the scale-factor round addition block section 51 to the ********** 28 number of steps as compared with the pixel spacing value GK=32 number of steps, the 1st shift signal S= 0 is supplied to selector 52B and the interpolation filter section 55 from comparator 52A. Here, selector 52B is outputted to the interpolation filter section 55 as it is in the scale-factor round addition block section 51 with the control signal of the 1st shift signal S= 0 by making the ********** 28 number of steps into the interpolation initial phase value XF=28 number of steps.

[0077] As shown in drawing 9 and drawing 11 , in the interpolation filter section 55, with therefore, the inputted 1st shift signal S= 0 to the 00th line Interpolation is started from the location where the pixel for interpolation initiation is the 00th pixel of the 00th line, and becomes the number of steps of interpolation initial phase value XF=28 with this 00th pixel as the starting point. Level distortion amendment is performed to the 00th line by carrying out pixel interpolation along with 00 lines every interpolation pixel spacing value HGK=56 number of steps from this interpolation initial valve position.

[0078] Next, since it is beforehand set as the adjacent pixel spacing value GK=32 number of steps, the interpolation initiation timing value-HS=-77 number of steps, and the interpolation pixel spacing value HGK=54 number of steps in the 01st line Like the 00th above-mentioned line, in the scale-factor round addition block section 51 by two round addition The output value from comparator 51C in this scale-factor round addition block section 51 will change to the number of steps of plus, namely, the number of steps of -HS+HGK+HGK=-77+54+54=31 is obtained in the scale-factor round addition block section 51.

[0079] Then, in the interpolation initial-valve-position detection block section 52, since the ********** 31 number of steps is smaller than the pixel spacing value GK=32 number of steps in the scale-factor round addition block section 51, the 1st shift signal S= 0 and the interpolation initial phase value XF=31 number of steps are outputted to the interpolation filter section 55 like the 00th above-mentioned line.

[0080] As shown in drawing 9 , in the interpolation filter section 55, with therefore, the inputted 1st shift signal S= 0 to the 01st line Interpolation is started from the location where the pixel for interpolation initiation is the 00th pixel of the 01st line, and becomes the interpolation initial phase value XF=31 number of steps with this 00th pixel as the starting point. Level distortion amendment is performed to the 01st line by carrying out pixel interpolation along with 01 lines

every interpolation pixel spacing value HGK=54 number of steps from this interpolation initial valve position.
[0081] Next, since it is beforehand set as the adjacent pixel spacing value GK=32 number of steps, the interpolation initiation timing value-HS=-70 number of steps, and the interpolation pixel spacing value HGK=52 number of steps in the 02nd line Like the 00th above-mentioned line and the 01st line, in the scale-factor round addition block section 51 by two round addition The output value from this scale-factor round addition block section 51 will change to the number of steps of plus, namely, the number of steps of -HS+HGK+HGK=-70+52+52=34 is obtained in the scale-factor round addition block section 51.
[0082] Then, at comparator 52A in the interpolation initial-valve-position detection block section 52, in the scale-factor round addition block section 51, since the ********** 34 number of steps is larger than the pixel spacing value GK in the scale-factor round addition block section 51 to the ********** 34 number of steps as compared with the pixel spacing value GK=32 number of steps, the 2nd shift signal S= 1 is supplied to selector 52B and the interpolation filter section 55 from comparator 52A. Here, selector 52B is outputted to the interpolation filter section 55 by making into the interpolation initial phase value XF=2 number of steps the number of steps of a result which subtracted [with the control signal of the 2nd shift signal S= 1] the pixel spacing value GK=32 number of steps to the ********** 34 number of steps in the scale-factor round addition block section 51 by subtractor 52C, i.e., the number of steps of 34-32=2.
[0083] As shown in drawing 9 and drawing 11 , in the interpolation filter section 55, with therefore, the inputted 2nd shift signal S= 1 to the 02nd line Interpolation is started from the location where the pixel for interpolation initiation is the 01st pixel of the 02nd line, and becomes the interpolation initial phase value XF=2 number of steps with this 01st pixel as the starting point. Level distortion amendment is performed to the 02nd line by carrying out pixel interpolation along with 02 lines every interpolation pixel spacing value HGK=52 number of steps from this interpolation initial valve position.
[0084] As described above, hereafter in the case of the 1st shift signal S= 0 Each Rhine starts pixel interpolation from the interpolation initial phase value XF over the 00th pixel. Level distortion amendment processing is performed for every interpolation pixel spacing value HGK of each Rhine. On the other hand, in the case of the 2nd CIF signal S= 1 Each Rhine started pixel interpolation from the interpolation initial phase value XF over the 01st pixel, carried out pixel interpolation for every interpolation pixel spacing value HGK one after another from this starting position, and has performed level distortion amendment processing.
[0085] Under the present circumstances, as shown in drawing 9 , along with the arrow head H which showed the interpolation starting position in each Rhine with the two-dot chain line, the 00th pixel turns into a pixel for interpolation initiation by the 00th line and the 01st line. The 01st pixel turns into a pixel for interpolation initiation to 02nd line - the 05th line, to 06th line - the 12th line, the 00th pixel turns into a pixel for interpolation initiation, and the image DHL for keystone distortion amendment as shown in drawing 4 (c) on the whole is memorized by the memory section 60 (drawing 3).
[0086] In addition, if level distortion amendment processing of each Rhine is performed as mentioned above to the center section of each Rhine and it carries out to bilateral symmetry centering on this center section, the image DHL for keystone distortion amendment as shown in drawing 4 (c) will be obtained.
[0087] Interpolation initiation timing value which starts interpolation virtually for every Rhine in the above-mentioned level distortion amendment processing section 50 - HS is changed. Change the interpolation initial phase value XF for every Rhine, and for every Rhine further by and the thing for which the interpolation pixel spacing value HGK equivalent to the level contraction scale factor to an image is changed, pixel interpolation is performed for every Rhine, and a horizontal keystone distortion is amended Since functionality can be given between the interpolation pixels which each horizontal Rhine adjoins, horizontal image quality degradation generated in simple pixel infanticide at the time of level distortion amendment processing in which it explained in the conventional example can be pressed down.

[0088] Although the perpendicular distortion amendment processing section 40 and the level distortion amendment processing section 50 mentioned the linear interpolation of two points as an example and explained generation of vertical interpolation Rhine, and horizontal pixel interpolation of each Rhine with the keystone distortion compensator concerning this invention explained in full detail above, it is applicable also to the four-point interpolation processing which increased the number of Rhine, and the number of pixels at the time of interpolation.
[0089] Furthermore, although it explained that keystone distortion amendment processing was performed according to the gate angle alpha (or beta), the perpendicular direction, the perpendicular contraction scale factor that receives horizontally, and level contraction scale factor to a screen 14 of a projector 10 when obtaining the image DHL for keystone distortion amendment It is also possible to perform keystone distortion amendment processing to the above and reverse according to the gate angle alpha (or beta), the perpendicular direction, the perpendicular magnifying power that receives horizontally, and level magnifying power to a screen 14 of a projector 10. Thus, what is necessary is just to perform level distortion amendment processing in the direction which accumulates input image data in memory in advance, and performs perpendicular distortion amendment processing in the direction which the number of Rhine increases from this memory according to perpendicular magnifying power, and the horizontal number of pixels increases according to level magnifying power, in performing keystone distortion amendment processing, expanding an image to input image data.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] When an image is expanded and projected on a screen from a projector, it is drawing for explaining the keystone distortion image produced on a screen.
[Drawing 2] It is drawing for explaining the amendment approach of the conventional keystone distortion image.
[Drawing 3] It is the block diagram having shown the whole keystone distortion compensator configuration concerning this invention.
[Drawing 4] In order to explain actuation by the whole keystone distortion compensator concerning this invention, it is drawing shown typically.
[Drawing 5] It is drawing having shown the fundamental view at the time of dividing between Rhine of the perpendicular direction in a liquid crystal panel, and between the horizontal pixels of each Rhine with a predetermined number at the time of perpendicular distortion amendment processing and level distortion amendment processing, and acquiring a vertical interpolation phase value and a vertical horizontal interpolation phase value by this division using the keystone distortion compensator concerning this invention.
[Drawing 6] In the keystone distortion compensator concerning this invention, it is the block diagram having shown the perpendicular distortion amendment processing section.
[Drawing 7] It is drawing for explaining interpolation Rhine at the time of the perpendicular distortion amendment processing section performing perpendicular distortion amendment processing.
[Drawing 8] In the keystone distortion compensator concerning this invention, it is the block diagram having shown the level distortion amendment processing section.
[Drawing 9] It is drawing for explaining the horizontal direct distortion amendment data at the time of the level distortion amendment processing section performing horizontal direct distortion amendment processing.
[Drawing 10] It is drawing having shown the horizontal direct distortion amendment data at the time of the level distortion amendment processing section performing horizontal direct distortion amendment processing on the chart.
[Drawing 11] It is drawing having shown the actuation which performs horizontal direct distortion amendment processing by the level distortion amendment processing section.
[Description of Notations]
10 [-- Projector lens,] -- A projector, 11 -- The light source, 12 -- A liquid crystal panel, 13 14 [-- Memory table,] -- A screen, 20 -- A keystone distortion compensator, 30 -- A control section, 31 40 -- The perpendicular distortion amendment processing section, 41 -- Interpolation filter sections 41 and 42 -- Rhine memory, 43 [-- Level distortion amendment processing section,] -- The interpolation data change-over section, 44 -- A line counter, 45 -- A comparator, 50 51 -- The scale-factor round addition block section, 52 -- Interpolation initial phase detection block section, 53 -- The level blanking detection block section, 54 -- Timing adjustment block section, 55 [-- Gate angle,] -- The interpolation filter section, 56 -- The Rhine memory, 60 -- The memory section, alpha, beta GK [-- A vertical interpolation phase value, X / -- A horizontal interpolation phase value, XF / -- A horizontal interpolation initial

phase value, S= 0 / -- The 1st shift signal, S= 1 / -- The 2nd shift signal.] -- A pixel spacing value, -HS -- A interpolation initiation timing value, HGK -- A interpolation pixel spacing value, Y

[Translation done.]

* NOTICES *

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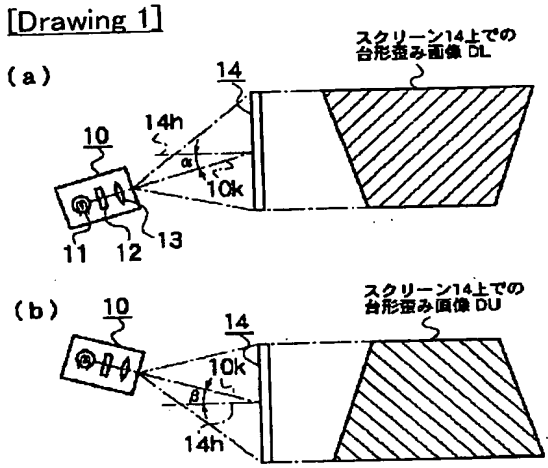
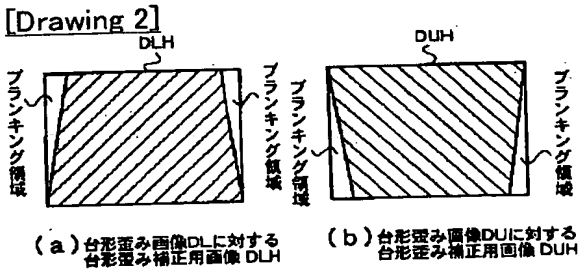
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

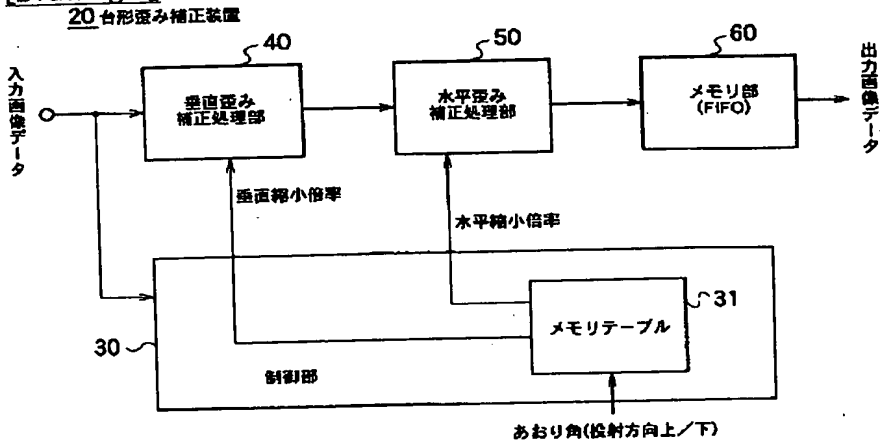
[Drawing 1]



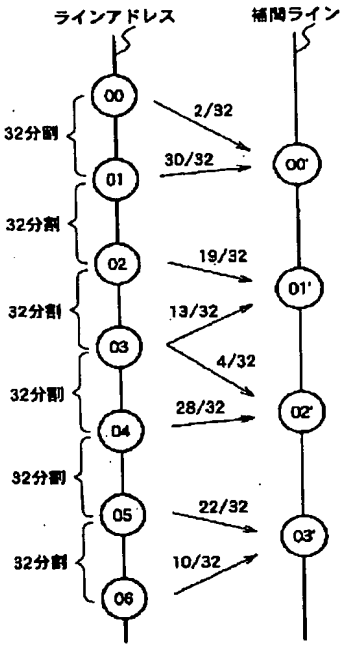
[Drawing 2]



[Drawing 3]

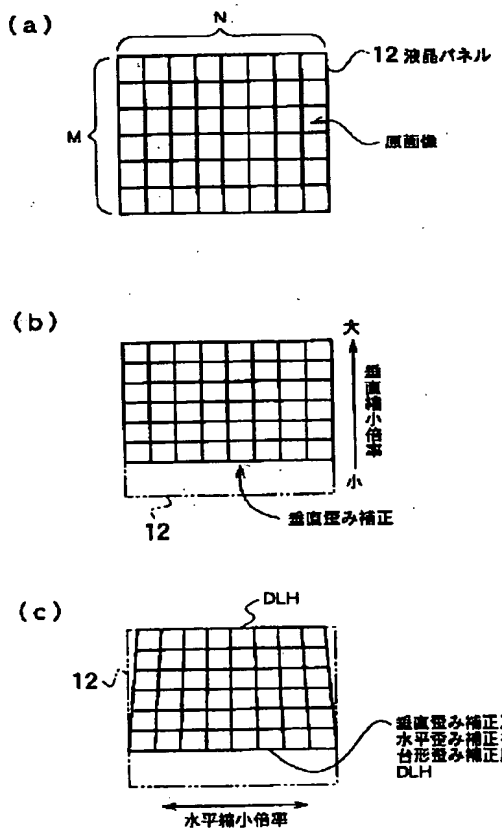


[Drawing 7]

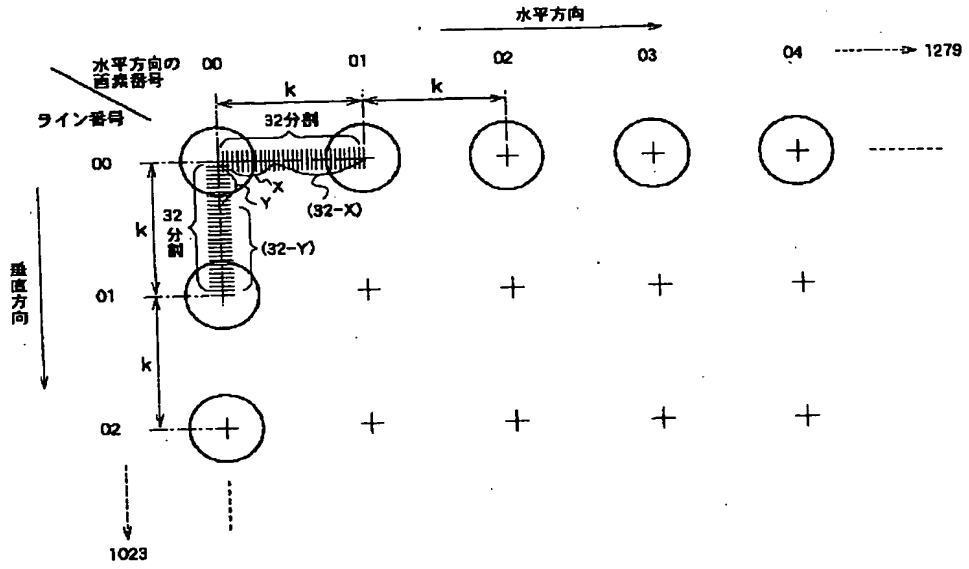


[Drawing 4]

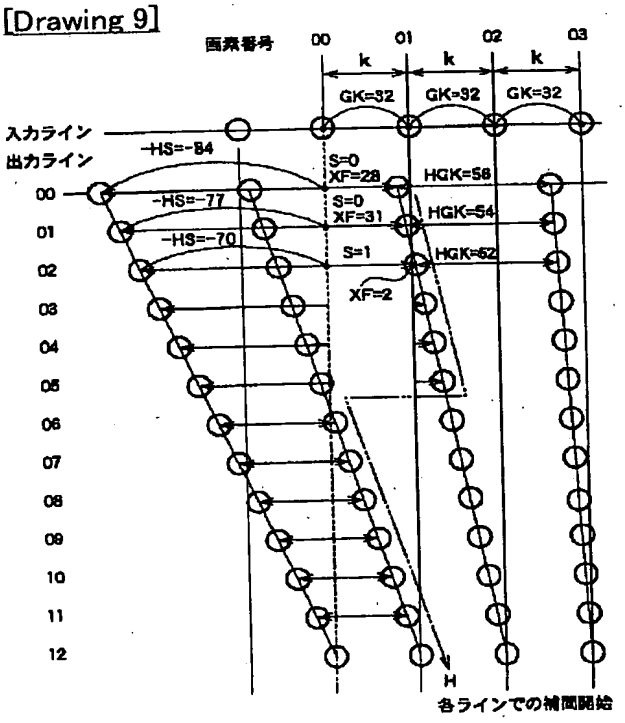
プロジェクタを床上に設置した時の台形歪み補正用画像を得るステップ



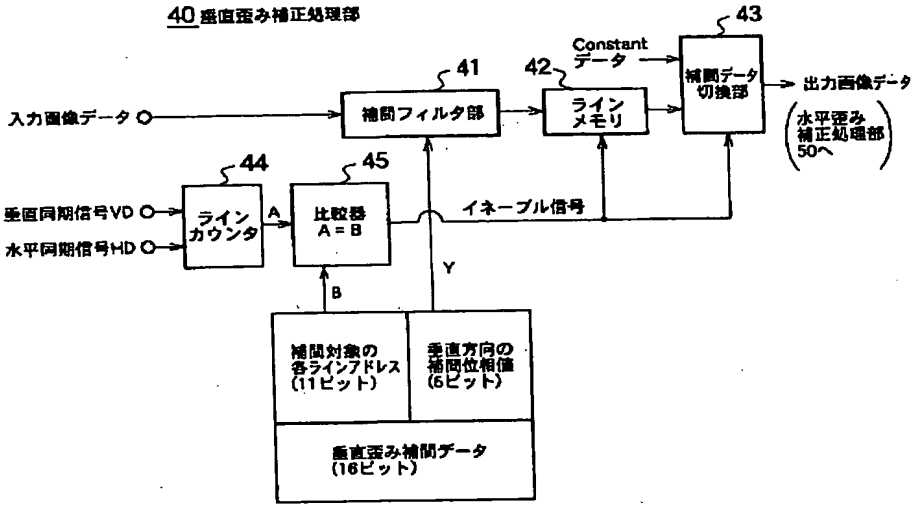
[Drawing 5]



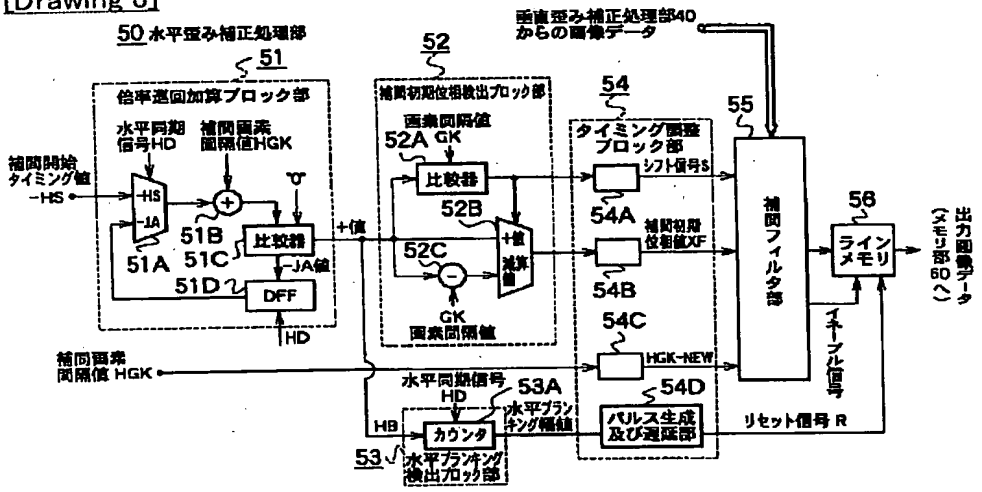
[Drawing 9]



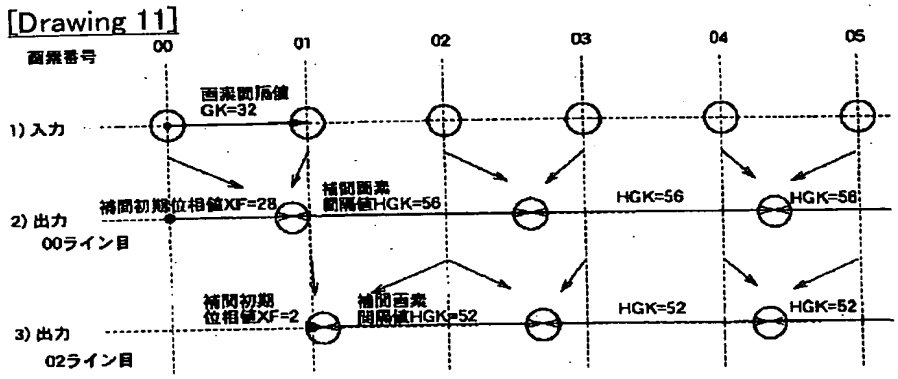
[Drawing 6]



[Drawing 8]



[Drawing 11]



[Drawing 10]

	メモリテーブル31に記憶した水平歪み補正データ					
ライン番号	画素間隔値 GK	補間開始タイミング値 -HS	補間画素間隔値 HGK	巡回回数 N	シフト信号 S	補間初期位相値 XF
00	32ステップ	-84ステップ	56ステップ	2	0	28ステップ
01	32ステップ	-77ステップ	54ステップ	2	0	31ステップ
02	32ステップ	-70ステップ	52ステップ	2	1	2ステップ
03	32ステップ	-63ステップ	50ステップ	2	1	5ステップ
04	32ステップ	-56ステップ	48ステップ	2	1	8ステップ
05	32ステップ	-49ステップ	46ステップ	2	1	11ステップ
06	32ステップ	-42ステップ	44ステップ	1	0	2ステップ
07	32ステップ	-35ステップ	42ステップ	1	0	7ステップ
08	32ステップ	-28ステップ	40ステップ	1	0	12ステップ
09	32ステップ	-21ステップ	38ステップ	1	0	17ステップ
10	32ステップ	-14ステップ	36ステップ	1	0	22ステップ
11	32ステップ	-7ステップ	34ステップ	1	0	27ステップ
12	32ステップ	0ステップ	32ステップ	0	0	0ステップ

[Translation done.]

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	1/133	505	1/133	505	5C006
G03B	21/00		G03B 21/00	D	5C058
G09G	3/20	621	G09G 3/20	621A	5C080

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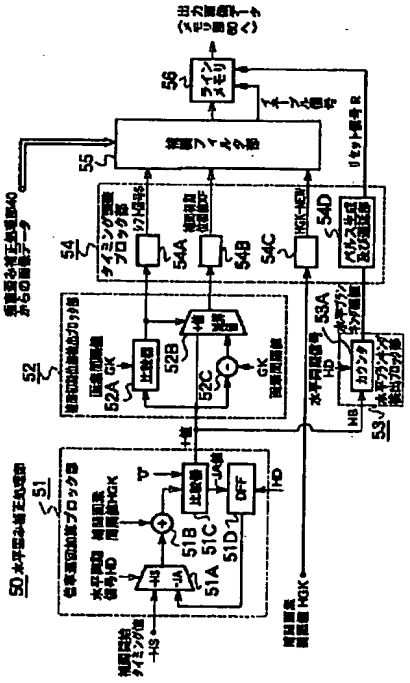
最終頁に続く

(54)【発明の名称】　台形歪み補正装置

(57)【要約】
【課題】　スクリーン上で生じる台形歪み画像を予め電気的に補正する。
【解決手段】　画像の水平方向の台形歪みを補正する際、液晶パネル１２内の水平方向の隣り合う画素間隔値ＧＫと、プロジェクタ１０へのあおり角α（又はβ）及び画像への水平縮小倍率又は水平拡大倍率とに応じて予めラインごとに設定され、且つ、各ラインの先頭画素よりもタイミングが早い時刻から画素補間を仮想的に開始するための補間開始タイミング値－ＨＳ及び隣り合う補間画素間の補間画素間隔値ＨＧＫとからなる水平歪み補正データとを入力して、補間開始タイミング値と補間画素間隔値とから各ラインの補間開始対象画素及びこの補間開始対象画素への補間初期位相値ＸＦを算出し、各ラインごとに補間開始対象画素への補間初期位相値の位置から次々と補間画素間隔値ごとに画素補間を行うための補間フィルタ部５５を有する水平歪み補正処理部５０とを備えた。



1

【特許請求の範囲】

【請求項１】　プロジェクタをスクリーンに対して斜め下方又は斜め上方に設置して、このプロジェクタ内の表示部材に表示した画像を前記スクリーン上に投射した時に該スクリーン上で生じる台形歪み画像を予め電気的に補正する台形歪み補正装置において、

前記画像の水平方向の台形歪みを補正する際、前記表示部材内の水平方向の隣り合う画素間隔値と、前記プロジェクタへのあおり角及び前記画像への水平縮小倍率又は水平拡大倍率とに応じて予めラインごとに設定され、且つ、各ラインの先頭画素よりもタイミングが早い時刻から画素補間を仮想的に開始するための補間開始タイミング値及び隣り合う補間画素間の補間画素間隔値とからなる水平歪み補正データとを入力して、前記補間開始タイミング値と前記補間画素間隔値とから各ラインの補間開始対象画素及びこの補間開始対象画素への補間初期位相値を算出し、各ラインごとに前記補間開始対象画素への前記補間初期位相値の位置から次々と前記補間画素間隔値ごとに画素補間を行うための補間フィルタ部を有する水平歪み補正処理部とを備えたことを特徴とする台形歪み補正装置。

【請求項２】　請求項１記載の台形歪み補正装置において、

前記水平歪み補正処理部は、水平同期信号のタイミングで取り込んだマイナス値である前記補間開始タイミング値に対して前記補間画素間隔値を該補間開始タイミング値がプラス値に転じるまで巡回加算して、プラス値を出力する倍率巡回加算ブロック部と、

前記倍率巡回加算ブロック部から出力されたプラス値が前記画素間隔値よりも小さい場合には、補間開始対象画素が先頭画素であることを指示する第１シフト信号を出力し、且つ、前記プラス値をそのまま前記先頭画素への前記補間初期位相値として出力する一方、前記プラス値が前記画素間隔値よりも大きい場合には、補間開始対象画素が先頭画素の次の画素であることを指示する第２シフト信号を出力し、且つ、前記プラス値から前記画素間隔値を引き算した値を前記次の画素への前記補間初期位相値として出力する補間初期位相検出ブロック部と、

前記補間初期位相検出ブロック部から出力された前記第１シフト信号又は前記第２シフト信号及び前記補間初期位相値と、前記補間画素間隔値とをそれぞれタイミング調整して前記補間フィルタ部へ出力するタイミング調整ブロック部とを備えたことを特徴とする台形歪み補正装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、プロジェクタをスクリーンに対して斜め下方又は斜め上方に設置して、このプロジェクタからの画像をスクリーン上に投射した時にスクリーン上で生じる台形歪み画像を予め電気的に補正する台形歪み補正装置に関するものである。

2

【０００２】

【従来の技術】ディジタル・マルチメディア時代の到来と共に、テレビジョン放送もディジタル化が加速され、既に放送が行われているＣＳディジタル放送とか、ごく最近放送が実用化されたＢＳディジタル放送などの画像をスクリーン上に拡大して投射でき、更に、高精細度のコンピュータ画像もスクリーン上に拡大して投射できるカラー液晶ライトバルブを備えたプロジェクタが注目されている。

【０００３】ここで、前方投射型のプロジェクタは、通常、スクリーンの前方側に置かれ、且つ、プロジェクタ自身の存在がスクリーン上に投射した画像への鑑賞の妨げにならないように、プロジェクタをスクリーンに対して斜め下方又は斜め上方に設置している。具体的には、例えば部屋の壁面に対して平行な状態にスクリーンが設置され、一方、プロジェクタはスクリーンの前方で床上或いは天井から吊り下げた状態に設置することが多い。なお、以下の説明において、プロジェクタを床上に設置した場合のように、スクリーンに対して下方側から画像を投射することを「下方からの投射」と呼び、逆に、プロジェクタを天井からつり下げた状態に設置した場合のように、スクリーンに対して上方側から画像を投射することを「上方からの投射」と呼ぶことにする。

【０００４】図１はプロジェクタから画像をスクリーン上に拡大して投射した時に、スクリーン上で生じる台形歪み画像を説明するための図であり、（ａ）は下方からの投射による台形歪み画像を示し、（ｂ）は上方からの投射による台形歪み画像を示した図、図２は従来の台形歪み画像の補正方法を説明するための図であり、（ａ），（ｂ）は図１（ａ），（ｂ）に示した台形歪み画像をそれぞれ電気的に補正する場合を示した図である。

【０００５】ここで、図１（ａ）に示した如く、カラー液晶ライトバルブを備えたプロジェクタ１０を床上に設置し、且つ、プロジェクタ１０内の光源１１からの光で表示部材となる液晶パネル１２に表示した画像を投射レンズ１３によりスクリーン１４上に拡大して投射した場合に、プロジェクタ１０の光軸１０ｋとスクリーン１４の中心位置の法線１４ｈとが一致せずに、プロジェクタ１０の光軸１０ｋとスクリーン１４の中心位置の法線１４ｈとの間にあおり角αが存在するために、スクリーン１４上には上辺の長さが底辺の長さより長い台形歪み（キーストーン歪み）画像ＤＬが発生する。

【０００６】一方、図１（ｂ）に示した如く、プロジェクタ１０を天井から吊り下げた状態に設置した場合にも、プロジェクタ１０の光軸１０ｋとスクリーン１４の中心位置の法線１４ｈとが一致せずに、プロジェクタ１０の光軸１０ｋとスクリーン１４の中心位置の法線１４ｈとの間にあおり角βが存在するために、スクリーン１

４上には上辺の長さが底辺の長さより短い台形歪み（キーストーン歪み）画像ＤＵが発生する。

【０００７】この際、プロジェクタ１０の設置状態によって変化するあおり角α，βに応じて台形歪み画像ＤＬ，ＤＵの発生状態も変化するものである。

【０００８】このようなことから、プロジェクタ１０の光軸１０ｋとスクリーン１４の中心位置の法線１４ｈとの間であおり角α（又はβ）が存在している場合において、スクリーン１４上に台形歪み画像ＤＬ（又はＤＵ）が生じないようにするために、従来より光学的な解決手法又は電気的な解決手法が各種提案されている。

【０００９】光学的な解決手法の代表的な例としては、プロジェクタ１０の投射光学系に、あおり機構（例えばあおりレンズ等）を設け、当該あおり機構によるあおり角を調整することにより、スクリーン１４上に発生する台形歪み画像ＤＬ（又はＤＵ）を補正するような解決手法が存在するものの、あおり機構などがコスト高となるために、下記する電気的な解決手法が採用されている。

【００１０】ここで、電気的な解決手法の代表的な一例としては、例えば、特開平５－３７８８０号公報に開示されているように、プロジェクタ１０内の液晶パネル１２に表示される投射前の原画像に対して例えば画素を間引いて、間引いた画素の分だけ両端にブランキング領域を付加している。

【００１１】即ち、プロジェクタ１０を床上に設置した下方からの投射の場合に、図２（ａ）に示したように、液晶パネル１２に表示される台形歪み補正用画像ＤＬＨは、図１（ａ）に示した台形歪み画像ＤＬに対して上下が逆な台形になるように各ラインごとに画素を間引いて圧縮して、間引いた画素の分だけ両端にブランキング領域を付加した状態で投射している。

【００１２】一方、プロジェクタ１０を天井から吊り下げて設置した上方からの投射の場合に、図２（ｂ）に示したように、液晶パネル１２に表示される台形歪み補正用画像ＤＵＨは、図１（ｂ）に示した台形歪み画像ＤＵに対して上下が逆な台形になるように各ラインごとに画素を間引いて圧縮して、間引いた画素の分だけ両端にブランキング領域を付加した状態で投射している。

【００１３】

【発明が解決しようとする課題】ところで、上記したように、プロジェクタ１０をスクリーン１４に対して斜め下方又は斜め上方に設置した時にスクリーン上で生じる台形歪み画像ＤＬ又はＤＵを、プロジェクタ１０内の液晶パネル１２に表示される原画像に対して予め電気的に補正する場合に、台形歪み補正処理した後の台形歪み補正用画像ＤＬＨ又はＤＵＨは、垂直方向に対して垂直縮小倍率に応じてライン数を間引いているにすぎないので垂直方向の隣り合うライン間で相関がなくなり、且つ、水平方向に対して各ラインごとに水平方向の画素数を間引いているにすぎないので隣り合う画素間でも相関がなくなるために、画素がずれた画像になり、画質を著しく劣化させた状態で台形歪み画像を電気的に補正することになり、スクリーン１４上で良好な画質の投射画像が得られない。

【００１４】また、近年、プロジェクタ等を使用して投射するソースとしては、我が国の標準テレビジョン方式の映像信号であるＮＴＳＣ信号（National Television System Committee）による標準画像のみならず、ＣＳディジタル放送やＢＳディジタル放送などによる高画質のディジタルカラー画像とか、パーソナルコンピュータで取り扱われる高精細度のコンピュータ画像などが用いられるようになっている。

【００１５】本来、台形歪み補正処理を電気的に行う場合には、垂直方向のライン単位の処理と、水平方向の画素単位（ドット単位）の処理とを同時に行う２次元処理が合理的であるが、例えばパーソナルコンピュータで取り扱われるコンピュータ画像の一つであるＳＸＧＡ（Super eXtended Graphics Array）画像は、垂直方向が１０２４ライン、水平方向が１２８０画素で矩形状の有効画像領域を形成し、且つ、ＳＸＧＡ信号の水平方向のクロック周波数が１００ＭＨｚ以上と高速になるため、台形歪み補正処理時に垂直方向及び水平方向を同時に２次元処理を行う場合に、とくに、水平方向の処理を画素単位（ドット単位）で高速に処理しなければならないため、大規模なあるいは複雑なハード構成を必要とするなどの問題がある。

【００１６】そこで、台形歪み補正処理を電気的に行う場合に、台形歪み補正処理した後の台形歪み補正用画像は、垂直方向の隣り合うライン間で相関があり、且つ、各ラインの水平方向の隣り合う画素間でも相関があり、しかも、垂直方向の補正処理と水平方向の補正処理とを別けて行うことで小規模なハード構成でも台形歪み補正を良好に行うことができる台形歪み補正装置が望まれている。

【００１７】

【課題を解決するための手段】本発明は上記課題に鑑みてなされたものであり、第１の発明は、プロジェクタをスクリーンに対して斜め下方又は斜め上方に設置して、このプロジェクタ内の表示部材に表示した画像を前記スクリーン上に投射した時に該スクリーン上で生じる台形歪み画像を予め電気的に補正する台形歪み補正装置において、前記画像の水平方向の台形歪みを補正する際、前記表示部材内の水平方向の隣り合う画素間隔値と、前記プロジェクタへのあおり角及び前記画像への水平縮小倍率又は水平拡大倍率とに応じて予めラインごとに設定され、且つ、各ラインの先頭画素よりもタイミングが早い時刻から画素補間を仮想的に開始するための補間開始タイミング値及び隣り合う補間画素間の補間画素間隔値とからなる水平歪み補正データとを入力して、前記補間開始タイミング値と前記補間画素間隔値とから各ラインの

補間開始対象画素及びこの補間開始対象画素への補間初期位相値を算出し、各ラインごとに前記補間開始対象画素への前記補間初期位相値の位置から次々と前記補間画素間隔値ごとに画素補間を行うための補間フィルタ部を有する水平歪み補正処理部とを備えたことを特徴とする台形歪み補正装置である。

【００１８】また、第２の発明は、上記した第１の発明の台形歪み補正装置において、前記水平歪み補正処理部は、水平同期信号のタイミングで取り込んだマイナス値である前記補間開始タイミング値に対して前記補間画素間隔値を該補間開始タイミング値がプラス値に転じるまで巡回加算して、プラス値を出力する倍率巡回加算ブロック部と、前記倍率巡回加算ブロック部から出力されたプラス値が前記画素間隔値よりも小さい場合には、補間開始対象画素が先頭画素であることを指示する第１シフト信号を出力し、且つ、前記プラス値をそのまま前記先頭画素への前記補間初期位相値として出力する一方、前記プラス値が前記画素間隔値よりも大きい場合には、補間開始対象画素が先頭画素の次の画素であることを指示する第２シフト信号を出力し、且つ、前記プラス値から前記画素間隔値を引き算した値を前記次の画素への前記補間初期位相値として出力する補間初期位相検出ブロック部と、前記補間初期位相検出ブロック部から出力された前記第１シフト信号又は前記第２シフト信号及び前記補間初期位相値と、前記補間画素間隔値とをそれぞれタイミング調整して前記補間フィルタ部へ出力するタイミング調整ブロック部とを備えたことを特徴とする台形歪み補正装置である。

【００１９】

【発明の実施の形態】以下に本発明に係る台形歪み補正装置の一実施例を、図１，図３乃至図１１を参照して、＜台形歪み補正装置の全体構成及び全体動作＞，＜垂直歪み補正処理部＞，＜水平歪み補正処理部＞の順に詳細に説明する。

【００２０】＜台形歪み補正装置の全体構成及び全体動作＞図３は本発明に係る台形歪み補正装置の全体構成を示したブロック図、図４は本発明に係る台形歪み補正装置の全体動作を説明するために模式的に示した図であり、（ａ）は原画像の画像配列を示し、（ｂ）は垂直歪み補正処理による画像配列を示し、（ｃ）は垂直歪み補正処理及び水平歪み補正処理を経て最終的に生成される台形歪み補正用画像の画像配列を示した図、図５は本発明に係る台形歪み補正装置を用いて、垂直歪み補正処理時及び水平歪み補正処理時に液晶パネル内の垂直方向のライン間及び各ラインの水平方向の画素間を所定数で分割して、この分割により垂直方向の補間位相値及び水平方向の補間位相値を得る際の基本的な考え方を示した図である。

【００２１】図３に示した如く、本発明に係る台形歪み補正装置２０は、カラー液晶ライトバルブなどを用いたプロジェクタ１０（図１）に適用され、このプロジェクタ１０をスクリーン１４（図１）に対して斜め下方又は斜め上方に設置して、プロジェクタ１０から画像をスクリーン１４上に拡大して投射した時にスクリーン１４上で生じる台形歪み画像を予め電気的に補正するものである。この際、プロジェクタ１０は斜め下方又は斜め上方に設置することで、スクリーン１４に対して図１（ａ）又は図１（ｂ）に示したあおり角α又はあおり角βが与えられており、このあおり角α又はあおり角βと、画像への垂直縮小倍率及び水平縮小倍率に応じて台形歪み補正用画像が得られるように構成されている。

【００２２】尚、画像への垂直縮小倍率及び水平縮小倍率に代えて、画像への垂直拡大倍率及び水平拡大倍率に応じて台形歪み補正用画像を得ることも可能であり、これについては後述する。

【００２３】上記した本発明に係る台形歪み補正装置２０は、入力画像データから垂直同期信号ＶＤ及び水平同期信号ＨＤなどを生成して装置全体の制御を行うと共に、画像の垂直方向を垂直縮小倍率に応じてライン数を間引きながら補間ラインを生成するための垂直歪み補正データと、画像の水平方向をラインごとの水平縮小倍率に応じて画素数を間引きながら画素補間するための水平歪み補正データとをプロジェクタ１０のスクリーン１４へのあおり角α（又はβ）に応じて記憶したメモリテーブル３１を備えた制御部３０と、プロジェクタ１０内の液晶パネル１２に表示する入力画像データに対して、垂直方向の台形歪み補正処理をライン単位で行う垂直歪み補正処理部４０と、垂直方向の台形歪み補正処理を行った後に水平方向の台形歪み補正処理を各ラインごとに画素単位（ドット単位）で行う水平歪み補正処理部５０と、垂直歪み補正処理及び水平歪み補正処理後の画像データを一時的に蓄積して、ここに蓄積した画像データを所定のタイミングで出力する先入れ先出し（ＦＩＦＯ）のメモリ部６０とから概略構成されている。

【００２４】この際、垂直歪み補正処理部４０と水平歪み補正処理部５０とに別けてそれぞれ独立して行うことにより、パーソナルコンピュータで取り扱われる際に高速処理が必要なＳＸＧＡ画像などに対して台形歪み補正処理の高速化とハード規模の小型化を実現している。

【００２５】また、垂直歪み補正処理部部４０は、垂直方向のライン数を垂直縮小倍率に従って間引きながらライン間隔を画素補間によりフィルタリング処理し、水平歪み補正処理部部５０は、各ラインの水平方向に画素数を水平縮小倍率に従って間引きながら画素間隔を画素補間によりフィルタリング処理することで、隣り合う上下のライン間に対して相関性を持たせ、且つ、各ラインの水平方向の隣り合う画素間でも相関性を持たせている。

【００２６】尚、上記構成による台形歪み補正装置２０では、入力画像データに対して垂直方向の台形歪み補正処理を先に行った後に水平方向の台形歪み補正処理を行

っているが、これに限ることなく、水平方向の台形歪み補正処理を先に行った後に垂直方向の台形歪み補正処理を行うように垂直歪み補正処理部と水平歪み補正処理部の順序を入れ替えて構成することも可能である。

【００２７】次に、プロジェクタ１０をスクリーン１４に対して例えば斜め下方の床上に設置した下方からの投射の場合において、垂直歪み補正処理と水平歪み補正処理の概念について、図４（ａ）～（ｃ）を用いて説明する。

【００２８】図４（ａ）に示した如く、液晶パネル１２内は垂直方向にMライン（M画素）、水平方向にN画素を有するものとし、この液晶パネル１２に入力画像データをそのまま表示した場合には、M×N個の画素による原画像が得られる。

【００２９】一方、図４（ｂ）に示した如く、入力画像データに対して台形歪み補正装置２０内の垂直歪み補正処理部４０により垂直方向の台形歪み補正処理をライン単位で行った場合には、液晶パネル１２の垂直方向のラインは下方から上方に向かって垂直縮小倍率が除々に増加した画像となる。

【００３０】更に、図４（ｃ）に示した如く、垂直方向の台形歪み補正処理を行った後に、水平歪み補正処理部５０により水平方向の台形歪み補正処理を各ラインごとに画素単位（ドット単位）で行った場合には、液晶パネル１２の水平方向の各画素は水平縮小倍率が下方が小さく、上方に向かうにつれて大きくなり、スクリーン上で生じた台形歪み画像を予め逆補正した状態の台形歪み補正用画像ＤＨＬが得られる。

【００３１】次に、台形歪み補正装置２０を用いて、垂直歪み補正処理時及び水平歪み補正処理時に液晶パネル１２内の垂直方向のライン間及び各ラインの水平方向の画素間を所定数で分割して、この分割により垂直方向の補間位相値及び水平方向の補間位相値を得る際の基本的な考え方について、先に図５を用いて述べておく。

【００３２】図５に示した如く、液晶パネル１２の矩形状の有効画像領域内には、ＳＸＧＡ画像に対応して垂直方向に１０２４ライン（１０２４画素）が設けられて各ラインにラインアドレスが１０ビット以上を用いて付与されている。一方、水平方向には１２８０画素が設けられていて各画素に対して画素番号が１１ビット以上を用いて付与されている。尚、水平方向は各ラインの中央部を中心にして左右対称に水平方向の画素補間処理が可能である。

【００３３】また、垂直方向のライン間隔（＝上下の画素間隔）及び各ラインの水平方向の隣り合う画素間隔は共に一定の間隔ｋに設定されており、且つ、一定の間隔ｋ内を所定数として例えば３２段階に分割することで、ｋ／３２を位相値への単位値（＝１ステップ値）として、この分割値を５ビットを用いたステップ数で表示している。

【００３４】そして、垂直方向に画素補間処理する時には、垂直方向の各ラインの画素データを起点として３２分割したうちの分割値Ｙを垂直方向の補間位相値として各ラインごとに設定すれば、一つのラインに対する位相値Ｙと、この一つのラインに一番近い次のラインまでの残りの分割値は（３２－Ｙ）となっている。

【００３５】同様、水平方向に画素補間処理する時には、各ラインの水平方向の各画素を起点として３２分割したうちの分割値Ｘを水平方向の補間位相値として各画素ごとに設定すれば、一つの画素に対する位相値Ｘと、この一つの画素に一番近い次の画素までの残り分割値は（３２－Ｘ）となっている。

【００３６】尚、実施例ではライン間及び画素間を所定数で分割する際に、ＳＸＧＡ画像に対応しては３２分割が良好であることを確認して設定したが、画像の画質精度に応じて分割数Ｎを適宜設定すれば良い。

【００３７】＜垂直歪み補正処理部＞図６は本発明に係る台形歪み補正装置において、垂直歪み補正処理部を示したブロック図、図７は垂直歪み補正処理部により垂直歪み補正処理を行った際の補間ラインを説明するための図である。

【００３８】図６に示した垂直歪み補正処理部４０は、本出願人から先に提案した特願平１１－３５９７４６号に基づくものであり、プロジェクタ１０（図１）により液晶パネル１２に表示される原画像をそのままスクリーン１４に拡大して投射した時に発生することになる台形歪み画像に対して、特に画像の垂直方向についての台形歪みを補正するための垂直歪み補正処理を入力画像データに対して施すために、補間フィルタ部４１と、ラインメモリ４２と、補間データ切換部４３と、ラインカウンタ４４と、比較器４５とを備えている。

【００３９】上記した垂直歪み補正処理部４０において、入力画像データは、補間フィルタ部４１に送られる。上記した補間フィルタ部４１は、入力画像データのうちで各ラインごとの垂直方向の画像データに対して補間位相値Ｙに基づいて補間ラインのデータを生成するための垂直フィルタを備えている。

【００４０】ここで、制御部３０（図３）はプロジェクタ１０のスクリーン１４へのあおり角α（又はβ）と、画像への垂直縮小倍率とに応じて画像の垂直方向のラインを補間する垂直歪み補正データとして、１１ビットを用いて表示される補間対象の各ラインアドレスＢと、各ラインアドレスＢと対をなして５ビットを用いて表示される垂直方向の補間位相値Ｙとをメモリテーブル３１（図３）から読み出して、各ラインアドレスＢを比較器４５に供給すると共に、垂直方向の補間位相値Ｙを補間フィルタ部４１に供給している。

【００４１】尚、この実施例では、メモリテーブル３１（図３）に記憶されている垂直歪み補正データは、プロジェクタ１０｛図１（ａ）｝による下方から投射時のあ

おり角αと、垂直縮小倍率とに応じて予め算出されたものである。

【００４２】また、制御部３０（図３）は入力画像データから垂直同期信号ＶＤ及び水平同期信号ＨＤを生成して、ここで生成した垂直同期信号ＶＤ及び水平同期信号ＨＤをラインカウンタ４４に供給している。そして、ラインカウンタ４４は、垂直同期信号ＶＤ及び水平同期信号ＨＤに基づいて入力画像データのライン数をカウントし、そのカウント値を入力ラインのアドレスＡとして比較器４５に送っている。

【００４３】上記した比較器４５は、ラインカウンタ４４から供給された入力ラインのアドレスＡ（カウント値）と、メモリテーブル３１（図３）から供給された補間対象の各ラインアドレスＢとを順次比較し、この比較の結果、両者のアドレス値が一致した時（Ａ＝Ｂの時）に、補間フィルタ部４１にて生成する補間ラインのデータが有効であることを示すイネーブル信号をラインメモリ４２と補間データ切換部４３とに知らせている。

【００４４】一方、補間フィルタ部４１には、メモリテーブル３１（図３）から補間対象の各ラインアドレスＢと対をなす垂直方向の補間位相値Ｙが順次供給されており、補間対象のラインアドレスＢのラインとこの近傍のラインとの間で補間位相値Ｙに基づいて補間ラインのデータが生成される。

【００４５】即ち、補間フィルタ部４１における入力画像データの補間ラインのデータを生成する方法として、図７を用いて２点の直線補間を例に挙げて説明する。ここで、２点の直線補間は、隣り合う上下のラインの画像データを補間位相値の比率に応じて演算して、この比率で隣り合う上下のラインを駆動することで、仮想的に補間ラインが生成されるものである。

【００４６】図７に示すように、入力画像データは、ラインアドレス００，０１，０２，……の順に、１水平ライン毎の画像データ［００］，［０１］，［０２］，……がライン単位で補間フィルタ部４１に順次入力される。

【００４７】そして、補間フィルタ部４１では、垂直方向の２点補間として、まず、補間対象の００ライン目の画像データ［００］と、０１ライン目の画像データ［０１］との間で補間演算を行う。この際、図５で説明したように、隣り合うライン間を例えば３２分割した場合、００ライン目の画像データ［００］に対して垂直方向の補間位相データとなる分割値Ｙは２ステップ数に予め設定されているので、次のラインまでの残りの分割値は（３２－Ｙ）ステップ数＝３０ステップ数となる。従って、補間フィルタ部４１で補間ラインの画像データ［００’］を生成する際に下記式の演算が行われる。［００’］＝（［００］×２＋［０１］×３０）÷３２

【００４８】次に、０１ライン目と０２ライン目との間では、補間対象のラインが設定されていないので、ラインが間引かれることになる。

【００４９】次に、補間対象の０２ライン目の画像データ［０２］と、０３ライン目の画像データ［０３］との間で補間演算を行う場合には、０２ライン目の画像データ［０２］に対して垂直方向の補間位相値となる分割値Ｙは１９ステップ数に予め設定されているので、次のラインまでの残りの分割値は（３２－Ｙ）ステップ数＝１３ステップ数となる。従って、補間フィルタ部４１で補間ラインの画像データ［０１’］を生成する際に下記式の演算が行われる。［０１’］＝（［０２］×１９＋［０３］×１３）÷３２

【００５０】以下、同様にして、ライン数が垂直縮小倍率に対応した補間対象の各ラインアドレスＢに従って間引かれながらライン間を補間することで、補間ラインの画像データ［００’］，［０１’］［０２’］，［０３’］，……の順で以降の各ラインについても補間ラインが生成される。

【００５１】そして、補間フィルタ部４１から出力された各補間ラインの画像データは、比較器４５からのイネーブル信号が出された都度にラインメモリ４２に一時的に蓄えられて、補間データ切換部４３に順次出力されている。

【００５２】次に、補間データ切換部４３では、比較器４５からのイネーブル信号が出された都度にラインメモリ４２から順次出力された補間ラインの画像データを後述する水平歪み補正処理部５０に出力する一方、イネーブル信号が出されない場合には任意に設定したｃｏｎｓｔａｎｔデータを水平歪み補正処理部５０側に出力している。この際、任意に設定したｃｏｎｓｔａｎｔデータは、垂直歪み補正処理で縮小された画像の有効ライン以外のラインをマスキングするためのデータである。そして、垂直歪み補正処理部４０により垂直歪み補正処理を行った画像データは先に説明した図４（ｂ）の状態が得られる。

【００５３】上記した水平歪み補正処理部５０では、画像への垂直縮小倍率に対応した補間対象のラインアドレスＢのラインと、この近傍のラインとの間で補間位相値Ｙに基づいて補間ラインを生成して垂直方向の台形歪みを補正することで、垂直方向の隣り合う補間ライン間で相関性を持たせることができるので、従来例で説明したような垂直歪み補正処理時に単純な画素間引きで発生する垂直方向の画質劣化を押さえることができる。

【００５４】＜水平歪み補正処理部＞図８は本発明に係る台形歪み補正装置において、水平歪み補正処理部を示したブロック図、図９は水平歪み補正処理部により水平直歪み補正処理を行う際の水平直歪み補正データを説明するための図、図１０は水平歪み補正処理部により水平直歪み補正処理を行う際の水平直歪み補正データを一覧表に示した図、図１１は水平歪み補正処理部により水平直歪み補正処理を行う動作を示した図である。

【００５５】図８に示した水平歪み補正処理部５０は、プロジェクタ１０（図１）により液晶パネル１２に表示される原画像をそのままスクリーン１４に拡大して投射した時に発生することになる台形歪み画像に対して、特に画像の水平方向についての台形歪みを補正するための水平歪み補正処理を垂直歪み補正処理部４０からの画像データに対して施すために、倍率巡回加算ブロック部５１と、補間初期位相検出ブロック部５２と、水平ブランキング検出ブロック部５３と、タイミング調整ブロック部５４と、補間フィルタ部５５と、ラインメモリ５６とを備えている。

【００５６】ここで、水平歪み補正処理部５０で水平歪み補正処理を施す際、図９に示したように、各ライン中で隣り合う画素間の一定の間隔ｋ内は前述したように例えば３２段階に分割されており、１／３２×ｋを単位ステップ数（＝１ステップ数）として以下説明すると、隣り合う画素間の画素間隔値ＧＫは各ライン共に３２ステップ数となり、且つ、この画素間隔値ＧＫは図１０に示したように制御部３０（図３）内のメモリテーブル３１に記憶されている。

【００５７】また、図９に示したように、各ライン中で先頭画素となる００番目の画素よりもタイミングが早い時刻から画素補間を仮想的に開始するものとすると、この補間開始タイミング値－ＨＳは、各ライン中の００番目の画素を起点としてマイナス（－）方向に向かって各ラインごとにマイナス値である補間開始タイミング値－ＨＳのステップ数がプロジェクタ１０｛図１（ａ）｝による下方から投射時のあおり角αに応じて予め設定されており、且つ、この補間開始タイミング値－ＨＳも図１０に示したように制御部３０（図３）内のメモリテーブル３１に記憶されている。

【００５８】また、各ラインごとに水平縮小倍率が予め設定されており、この水平縮小倍率は、図９に示したように、各ライン中で水平方向に画素補間した補間画素間隔値ＨＧＫに置換して表示されている。そして、各ラインの補間画素間隔値ＨＧＫのステップ数がプロジェクタ１０のあおり角αに応じて予め設定されており、且つ、この補間画素間隔値ＨＧＫも図１０に示したように制御部３０（図３）内のメモリテーブル３１に記憶されている。ここで、補間画素間隔値ＨＧＫと画素間隔値ＨＧＫとが一致している場合には水平縮小倍率は１であり、補間画素間隔値ＨＧＫが画素間隔値ＨＧＫよりも大きくなればなるほど水平縮小倍率が大きくなり、水平縮小倍率が大きくなればなるほど水平方向の画素数が多く間引かれて画素補間が行われることになる。

【００５９】また、各ライン中で水平方向に画素補間する際に、各画素に対する水平方向の補間位相値Ｘのうちで、最初の補間対象画素に対する補間位相値を補間初期位相値ＸＦと以下呼称すると、最初の補間対象画素は、後述するように先頭画素となる００番目の画素か、あるいは、先頭画素の次の画素となる０１番目の画素のいずれかであり、この時の水平方向の補間初期位相値ＸＦは図８に示した水平歪み補正処理部５０内の倍率巡回加算ブロック部５１と、補間初期位相検出ブロック部５２とにより算出されるようになっている。

【００６０】この際、水平歪み補正処理時に、各ライン中で補間対象の各画素に対する補間位相値Ｘを予め算出してメモリに記憶させ、補間対象の画素とこの近傍の画素との間で補間位相値Ｘに基づいて各画素ごとに画素補間を行う方法でも同じ結果が得られるものの、この方法を採用するとメモリ容量が莫大となるため、この実施例では、各ラインの補間初期位相値ＸＦと、この補間初期位相値ＸＦを起点として、同一ライン中では同じ間隔で画素補間をするための補間画素間隔値ＨＧＫとを記憶させることでメモリ容量を削減している。

【００６１】図８に戻り、水平歪み補正処理部５０内の倍率巡回加算ブロック部５１は、セレクタ５１Ａと、加算器５１Ｂと、比較器５１Ｃと、ＤＦＦ（Ｄフリップフロップ）５１Ｄとで巡回加算を行うように構成されている。

【００６２】そして、倍率巡回加算ブロック部５１のセレクタ５１Ａには、制御部３０（図３）内のメモリテーブル３１から各ラインごとに読み出された補間開始タイミング値－ＨＳがマイナス値のステップ数として入力される。上記したセレクタ５１Ａは、入力された補間開始タイミング値－ＨＳと下記する巡回加算値－ＪＡとのいずれかを水平同期信号ＨＤのタイミングで選択して、選択した一方の値－ＨＳ又は－ＪＡを加算器５１Ｂに供給している。

【００６３】次に、加算器５１Ｂには、制御部３０（図３）内のメモリテーブル３１から各ラインごとに読み出された補間画素間隔値ＨＧＫが入力されており、この補間画素間隔値ＨＧＫは前述したように各ラインの水平縮小倍率に応じてステップ数が予め設定されたものである。そして、加算器５１Ｂでは、セレクタ５１Ａで選択した一方の値－ＨＳ又は－ＪＡに補間画素間隔値ＨＧＫを加算して、加算結果を比較器５１Ｃに入力し、比較器５１Ｃでここに予め入力した０値に対して加算結果を比較して加算結果が０値以上のプラス値のステップ数に転じたらこのプラス値のステップ数を補間初期位相検出ブロック部５２と水平ブランキング検出ブロック部５３とに出力する一方、加算結果が０値より小さいマイナス値となった巡回加算値－ＪＡのステップ数であればＤＦＦ（Ｄフリップフロップ）５１Ｄを介して加算結果をセレクタ５１Ａに戻し、加算器５１Ｂの加算結果がプラス値に転じるまで巡回加算される。この際、補間画素間隔値ＨＧＫを何回加えることで加算結果がプラス値に転じるかを示すために巡回回数Ｎが図１０に示した如く計数できる。

【００６４】即ち、セレクタ５１Ａは、補間開始タイミ

ング値－ＨＳが入力された時にはこの補間開始タイミング値－ＨＳを加算器５１Ｂに供給して、加算器５１Ｂで補間開始タイミング値－ＨＳと補間画素間隔値ＨＧＫとを加算して、この加算結果がマイナス値の巡回加算値－ＪＡであれば、この巡回加算値－ＪＡがセレクタ５１Ａに巡回されて次のタイミングでセレクタ５１Ａは巡回加算値－ＪＡを選択し、加算器５１Ｂでの加算結果が比較器５１Ｃでプラス値のステップ数に転じるまで巡回加算を繰り返すことになる。従って、比較器５１から出力されるプラス値のステップ数は、各ラインの００番目の画素を起点としてマイナス方向に設定した補間開始タイミング値－ＨＳとは逆の方向で、００番目の画素を起点してプラス方向のステップ数の値が得られることになる。

【００６５】次に、水平歪み補正処理部５０内の補間初期位相検出ブロック部５２は、比較器５２Ａと、セレクタ５２Ｂと、減算器５２Ｃとで構成されている。

【００６６】ここで、補間初期位相検出ブロック部５２内の比較器５２Ａ及びセレクタ５２Ｂ並びに減算器５２Ｃには、倍率巡回加算ブロック部５１の比較器５１Ｃから出力されたプラス値のステップ数が入力される。更に、補間初期位相検出ブロック部５２内の比較器５２Ａ及び減算器５２Ｃには、制御部３０（図３）内のメモリテーブル３１から読み出された画素間隔値ＧＫとして３２ステップ数が予め入力されている。

【００６７】ここで、補間初期位相検出ブロック部５２の比較器５２Ａでは、予め入力した画素間隔値ＧＫ＝３２ステップ数に対して、倍率巡回加算ブロック部５１の比較器５１Ｃから出力されたプラス値のステップ数が画素間隔値ＧＫ＝３２ステップ数より大きいか否かを問い、このプラス値のステップ数が画素間隔値ＧＫよりも小さい場合には第１シフト信号Ｓ＝０を出力し、大きい場合には第２シフト信号Ｓ＝１を出力し、この第１シフト信号Ｓ＝０又は第２シフト信号Ｓ＝１でセレクタ５２Ｂを制御すると共に、更に、第１シフト信号Ｓ＝０又は第２シフト信号Ｓ＝１をタイミング調整ブロック部５４内のタイミング調整器５４Ａを介してタイミング調整して補間フィルタ部５５に入力している。

【００６８】この際、補間フィルタ部５５に入力される第１シフト信号Ｓ＝０又は第２シフト信号Ｓ＝１は、補間開始対象画素を設定するための制御信号として機能しており、第１シフト信号Ｓ＝０が入力された場合には補間開始対象画素は各ライン共に００番目の画素となり、一方、第２シフト信号Ｓ＝１が入力された場合には補間開始対象画素は各ライン共に０１番目の画素となるものである。

【００６９】また、第１シフト信号Ｓ＝０がセレクタ５２Ｂに供給された時に、セレクタ５２Ｂは倍率巡回加算ブロック部５１の比較器５１Ｃから出力された画素間隔値ＧＫ＝３２ステップ数より小さいプラス値のステップ数をそのままセレクタ５２Ｂからタイミング調整ブロック部５４内のタイミング調整器５４Ｂを介してタイミング調整して、画素間隔値ＧＫ＝３２ステップ数より小さいプラス値のステップ数を水平方向の補間初期位相値ＸＦとして補間フィルタ部５５に入力しており、ここで得られた水平方向の補間初期位相値ＸＦは補間開始対象画素として上記したように００番目の画素に対応するものである。

【００７０】一方、第２シフト信号Ｓ＝１がセレクタ５２Ｂに供給された時に、セレクタ５２Ｂは減算器５２Ｃに入力した倍率巡回加算ブロック部５１の比較器５１Ｃから出力された画素間隔値ＧＫ＝３２ステップ数より大きいプラス値のステップ数から画素間隔値ＧＫ＝３２ステップ数を引き算して、画素間隔値ＧＫ＝３２ステップ数より小さくなった引き算結果のステップ数をタイミング調整ブロック部５４内のタイミング調整器５４Ｂを介してタイミング調整して、引き算した結果のステップ数を水平方向の補間初期位相値ＸＦとして補間フィルタ部５５に入力しており、ここで得られた水平方向の補間初期位相値ＸＦは補間開始対象画素として上記したように０１番目の画素に対応するものである。

【００７１】また、制御部３０（図３）内のメモリテーブル３１から各ラインごとに読み出された補間画素間隔値ＨＧＫは、タイミング調整ブロック部５４内のタイミング調整器５４Ｃを介してタイミング調整して、タイミング調整後の新たな補間画素間隔値ＨＧＫ－ＮＥＷとして補間フィルタ部５５に入力している。この際、タイミング調整後の新たな補間画素間隔値ＨＧＫ－ＮＥＷは、メモリテーブル３１に記憶された補間画素間隔値ＨＧＫのステップ数と同じステップ数であり、単にタイミング調整がなされたものである。

【００７２】また、倍率巡回加算ブロック部５１内の比較器５１Ｃから出力された０値以上（プラス値）のステップ数が水平ブランキング幅生成制御信号ＨＢとして水平ブランキング検出ブロック部５３内のカウンタ５３Ａに入力され、且つ、このカウンタ５３Ａに水平同期信号ＨＤも入力されている。そして、カウンタ５３Ａは水平同期信号ＨＤのタイミングでリセットされて、水平ブランキング幅生成制御信号ＨＢによりカウントを停止することで、各ラインごとに倍率巡回加算ブロック部５１内の比較器５１Ｃから出力された０値以上（プラス値）のステップ数を水平ブランギング幅値として算出して、タイミング調整ブロック部５４内のパルス生成及び遅延部５４Ｄに供給している。この後、タイミング調整ブロック部５４内のパルス生成及び遅延部５４Ｄでは、水平ブランギング幅値に基づいてラインメモリ５６へのリセット信号Ｒを生成している。

【００７３】上記から、補間フィルタ部５５では、第１シフト信号Ｓ＝０又は第２シフト信号Ｓ＝１，水平方向の補間初期位相値ＸＦ，タイミング調整後の新たな補間画素間隔値ＨＧＫ－ＮＥＷに基づいて、垂直歪み補正処

理部４０から出力した画像データに対して各ラインごとに画素補間することにより水平歪み補正処理を施して、イネーブル信号が出力された時に各ラインごとにラインメモリ５６に一時的に蓄積し、この後、ラインメモリ５６から各ラインの画像データを図３に示したメモリ部（ＦＩＦＯ）６０に順次蓄積しており、以下、具体的に説明する。

【００７４】図９及び図１０に示したように、プロジェクタ１０｛図１（ａ）｝の下方からの投射時のあおり角αと、画像への水平縮小倍率とに応じて、制御部３０（図３）内のメモリテーブル３１には水平歪み補正データとして画素間隔値ＧＫ，補間開始タイミング値－ＨＳ，補間画素間隔値ＨＧＫが予め記憶されている。

【００７５】まず、００ライン目では、隣り合う画素間隔値ＧＫ＝３２ステップ数、補間開始タイミング値－ＨＳ＝－８４ステップ数、補間画素間隔値ＨＧＫ＝５６ステップ数に予め設定されているので、図８に示した倍率巡回加算ブロック部５１で２回の巡回加算により、この倍率巡回加算ブロック部５１内の比較器５１Ｃからの出力値がプラスのステップ数に転じることになり、即ち、－ＨＳ＋ＨＧＫ＋ＨＧＫ＝－８４＋５６＋５６＝２８のステップ数が倍率巡回加算ブロック部５１で得られる。

【００７６】この後、図８に示した補間初期位置検出ブロック部５２内の比較器５２Ａでは、倍率巡回加算ブロック部５１で得らえられた２８ステップ数に対して、画素間隔値ＧＫ＝３２ステップ数と比較して、倍率巡回加算ブロック部５１で得らえられた２８ステップ数が画素間隔値ＧＫより小さいので、比較器５２Ａから第１シフト信号Ｓ＝０がセレクタ５２Ｂと補間フィルタ部５５とに供給される。ここで、セレクタ５２Ｂは第１シフト信号Ｓ＝０の制御信号により倍率巡回加算ブロック部５１で得らえられた２８ステップ数をそのまま補間初期位相値ＸＦ＝２８ステップ数として補間フィルタ部５５に出力する。

【００７７】従って、図９及び図１１に示した如く、補間フィルタ部５５では００ライン目に対して、入力された第１シフト信号Ｓ＝０により、補間開始対象画素が００ライン目の００番目の画素であり、この００番目の画素を起点として補間初期位相値ＸＦ＝２８のステップ数になる位置から補間を開始し、この補間初期位置から補間画素間隔値ＨＧＫ＝５６ステップ数ごとに００ラインに沿って画素補間をすることで００ライン目に対して水平歪み補正が行われる。

【００７８】次に、０１ライン目では、隣り合う画素間隔値ＧＫ＝３２ステップ数、補間開始タイミング値－ＨＳ＝－７７ステップ数、補間画素間隔値ＨＧＫ＝５４ステップ数に予め設定されているので、上記した００ライン目と同様に、倍率巡回加算ブロック部５１で２回の巡回加算により、この倍率巡回加算ブロック部５１内の比較器５１Ｃからの出力値がプラスのステップ数に転じることになり、即ち、－ＨＳ＋ＨＧＫ＋ＨＧＫ＝－７７＋５４＋５４＝３１のステップ数が倍率巡回加算ブロック部５１で得られる。

【００７９】この後、補間初期位置検出ブロック部５２では、倍率巡回加算ブロック部５１で得らえられた３１ステップ数が画素間隔値ＧＫ＝３２ステップ数より小さいので、上記した００ライン目と同様に、第１シフト信号Ｓ＝０と、補間初期位相値ＸＦ＝３１ステップ数とが補間フィルタ部５５に出力される。

【００８０】従って、図９に示した如く、補間フィルタ部５５では０１ライン目に対して、入力された第１シフト信号Ｓ＝０により、補間開始対象画素が０１ライン目の００番目の画素であり、この００番目の画素を起点として補間初期位相値ＸＦ＝３１ステップ数になる位置から補間を開始し、この補間初期位置から補間画素間隔値ＨＧＫ＝５４ステップ数ごとに０１ラインに沿って画素補間をすることで０１ライン目に対して水平歪み補正が行われる。

【００８１】次に、０２ライン目では、隣り合う画素間隔値ＧＫ＝３２ステップ数、補間開始タイミング値－ＨＳ＝－７０ステップ数、補間画素間隔値ＨＧＫ＝５２ステップ数に予め設定されているので、上記した００ライン目及び０１ライン目と同様に、倍率巡回加算ブロック部５１で２回の巡回加算により、この倍率巡回加算ブロック部５１からの出力値がプラスのステップ数に転じることになり、即ち、－ＨＳ＋ＨＧＫ＋ＨＧＫ＝－７０＋５２＋５２＝３４のステップ数が倍率巡回加算ブロック部５１で得られる。

【００８２】この後、補間初期位置検出ブロック部５２内の比較器５２Ａでは、倍率巡回加算ブロック部５１で得らえられた３４ステップ数に対して、画素間隔値ＧＫ＝３２ステップ数と比較して、倍率巡回加算ブロック部５１で得らえられた３４ステップ数が画素間隔値ＧＫより大きいので、比較器５２Ａから第２シフト信号Ｓ＝１がセレクタ５２Ｂと補間フィルタ部５５とに供給される。ここで、セレクタ５２Ｂは第２シフト信号Ｓ＝１の制御信号により減算器５２Ｃで倍率巡回加算ブロック部５１で得らえられた３４ステップ数に対して画素間隔値ＧＫ＝３２ステップ数を引き算した結果のステップ数、即ち、３４－３２＝２のステップ数を補間初期位相値ＸＦ＝２ステップ数として補間フィルタ部５５に出力する。

【００８３】従って、図９及び図１１に示した如く、補間フィルタ部５５では０２ライン目に対して、入力された第２シフト信号Ｓ＝１により、補間開始対象画素が０２ライン目の０１番目の画素であり、この０１番目の画素を起点として補間初期位相値ＸＦ＝２ステップ数になる位置から補間を開始し、この補間初期位置から補間画素間隔値ＨＧＫ＝５２ステップ数ごとに０２ラインに沿って画素補間をすることで０２ライン目に対して水平歪

み補正が行われる。

【００８４】以下、上記したように、第１シフト信号Ｓ＝０の場合は、各ライン共に、００番目の画素に対する補間初期位相値ＸＦから画素補間を開始して、各ラインの補間画素間隔値ＨＧＫごとに水平歪み補正処理を施し、一方、第２シフ信号Ｓ＝１の場合は、各ライン共に、０１番目の画素に対する補間初期位相値ＸＦから画素補間を開始して、この開始位置から次々と補間画素間隔値ＨＧＫごとに画素補間して水平歪み補正処理を施している。

【００８５】この際、図９に示したように、各ラインでの補間開始位置は二点鎖線で示した矢印Ｈに沿って００ライン目及び０１ライン目では００番目の画素が補間開始対象画素になり、０２ライン目～０５ライン目までは０１番目の画素が補間開始対象画素になり、０６ライン目～１２ライン目までは００番目の画素が補間開始対象画素になり、全体的には図４（ｃ）に示したような台形歪み補正用画像ＤＨＬがメモリ部６０（図３）に記憶される。

【００８６】尚、各ラインの水平歪み補正処理は、各ラインの中央部まで上記のように行い、この中央部を中心に左右対称に行えば図４（ｃ）に示したような台形歪み補正用画像ＤＨＬが得られるものである。

【００８７】上記した水平歪み補正処理部５０では、ラインごとに補間を仮想的に開始する補間開始タイミング値－ＨＳを変え、且つ、ラインごとに補間初期位相値ＸＦを変え、更に、ラインごとに画像への水平縮小倍率と等価である補間画素間隔値ＨＧＫを変えて各ラインごとに画素補間を施して水平方向の台形歪みを補正することで、水平方向の各ラインの隣り合う補間画素間で相関性を持たせることができるので、従来例で説明したような水平歪み補正処理時に単純な画素間引きで発生する水平方向の画質劣化を押さえることができる。

【００８８】以上詳述した本発明に係る台形歪み補正装置では、垂直歪み補正処理部４０及び水平歪み補正処理部５０共に、２点の直線補間を例として挙げて垂直方向の補間ラインの生成及び各ラインの水平方向の画素補間を説明したが、補間時にライン数，画素数を増やした４点補間処理にも応用可能である。

【００８９】更に、台形歪み補正用画像ＤＨＬを得る際に、プロジェクタ１０のスクリーン１４へのあおり角α（又はβ）と、垂直方向及び水平方向に対する垂直縮小倍率及び水平縮小倍率とに応じて台形歪み補正処理を行うように説明したが、上記と逆に、プロジェクタ１０のスクリーン１４へのあおり角α（又はβ）と、垂直方向及び水平方向に対する垂直拡大倍率及び水平拡大倍率とに応じて台形歪み補正処理を施すことも可能である。このように、入力画像データに対して画像を拡大しながら台形歪み補正処理を行う場合には、入力画像データを事前にメモリに蓄積しておき、このメモリから垂直拡大倍率に応じてライン数が増加する方向に垂直歪み補正処理を施し、且つ、水平拡大倍率に応じて水平方向の画素数が増加する方向に水平歪み補正処理を施せば良いものである。

【００９０】

【発明の効果】以上詳述した本発明に係る台形歪み補正回路によると、とくに、水平歪み補正処理部では、ラインごとに補間を仮想的に開始する補間開始タイミング値を変え、且つ、ラインごとに補間初期位相値を変え、更に、ラインごとに画像への水平縮小倍率又は垂直拡大倍率と等価である補間画素間隔値を変えて各ラインごとに画素補間を施して水平方向の台形歪みを補正することで、水平方向の各ラインの隣り合う補間画素間で相関性を持たせることができるので、従来例で説明したような水平歪み補正処理時に単純な画素間引きで発生する水平方向の画質劣化を押さえることができる。また、水平歪み補正処理部では、画素間隔値と、各ラインの補間開始タイミング値と補間画素間隔値とをメモリテーブルに記憶させておけば良いので、メモリテーブルの記憶容量を小さくすることができる。

【図面の簡単な説明】

【図１】プロジェクタから画像をスクリーン上に拡大して投射した時に、スクリーン上で生じる台形歪み画像を説明するための図である。

【図２】従来の台形歪み画像の補正方法を説明するための図である。

【図３】本発明に係る台形歪み補正装置の全体構成を示したブロック図である。

【図４】本発明に係る台形歪み補正装置の全体動作を説明するために模式的に示した図である。

【図５】本発明に係る台形歪み補正装置を用いて、垂直歪み補正処理時及び水平歪み補正処理時に液晶パネル内の垂直方向のライン間及び各ラインの水平方向の画素間を所定数で分割して、この分割により垂直方向の補間位相値及び水平方向の補間位相値を得る際の基本的な考え方を示した図である。

【図６】本発明に係る台形歪み補正装置において、垂直歪み補正処理部を示したブロック図である。

【図７】垂直歪み補正処理部により垂直歪み補正処理を行った際の補間ラインを説明するための図である。

【図８】本発明に係る台形歪み補正装置において、水平歪み補正処理部を示したブロック図である。

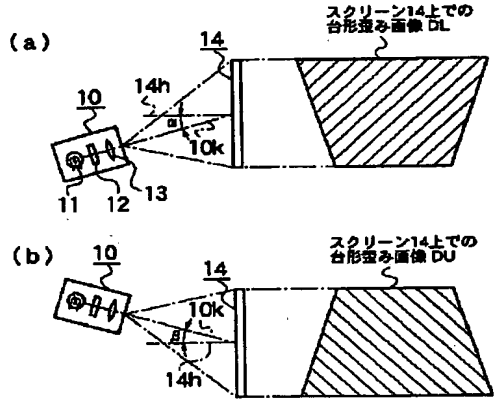
【図９】水平歪み補正処理部により水平直歪み補正処理を行う際の水平直歪み補正データを説明するための図である。

【図１０】水平歪み補正処理部により水平直歪み補正処理を行う際の水平直歪み補正データを一覧表に示した図である。

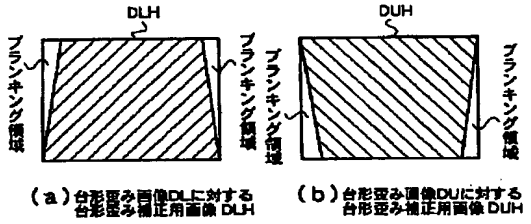
【図１１】水平歪み補正処理部により水平直歪み補正処理を行う動作を示した図である。

【符号の説明】
１０…プロジェクタ、１１…光源、１２…液晶パネル、１３…投射レンズ、１４…スクリーン、２０…台形歪み補正装置、３０…制御部、３１…メモリテーブル、４０…垂直歪み補正処理部、４１…補間フィルタ部４１、４２…ラインメモリ、４３…補間データ切換部、４４…ラインカウンタ、４５…比較器、５０…水平歪み補正処理部、５１…倍率巡回加算ブロック部、５２…補間初期位相検出ブロック部、５３…水平ブランキング検出ブロック部、５４…タイミング調整ブロック部、５５…補間フィルタ部、５６…ラインメモリ、６０…メモリ部、α，β…あおり角、ＧＫ…画素間隔値、－ＨＳ…補間開始タイミング値、ＨＧＫ…補間画素間隔値、Ｙ…垂直方向の補間位相値、Ｘ…水平方向の補間位相値、ＸＦ…水平方向の補間初期位相値、Ｓ＝０…第１シフト信号、Ｓ＝１…第２シフト信号。

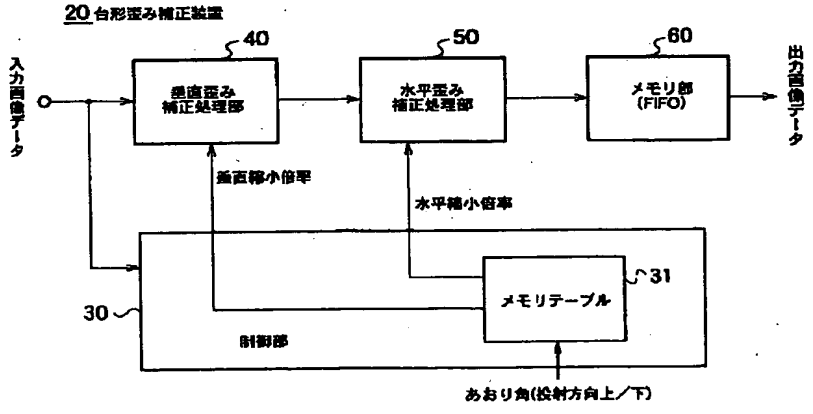
【図１】



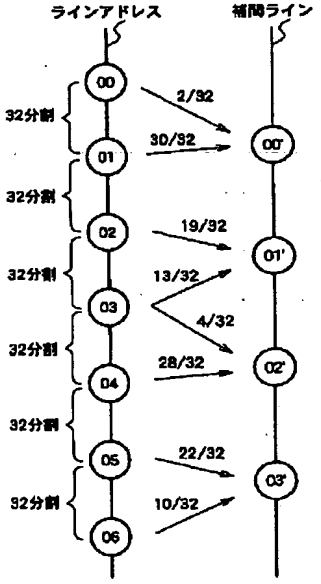
【図２】



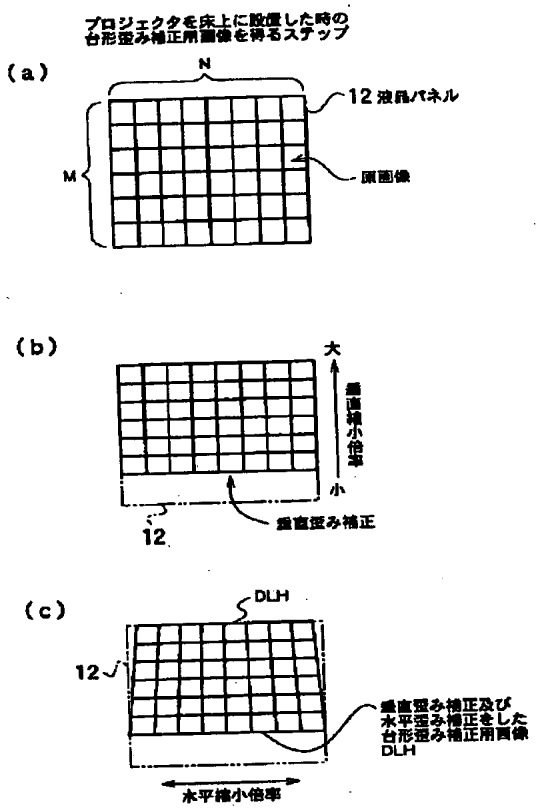
【図３】



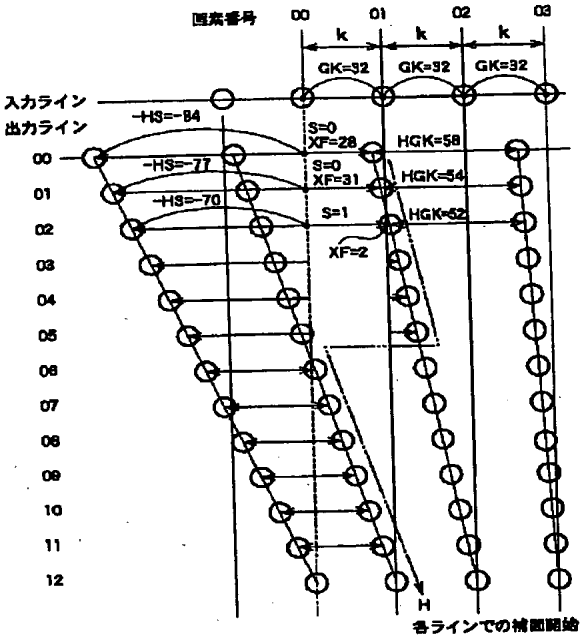
【図７】



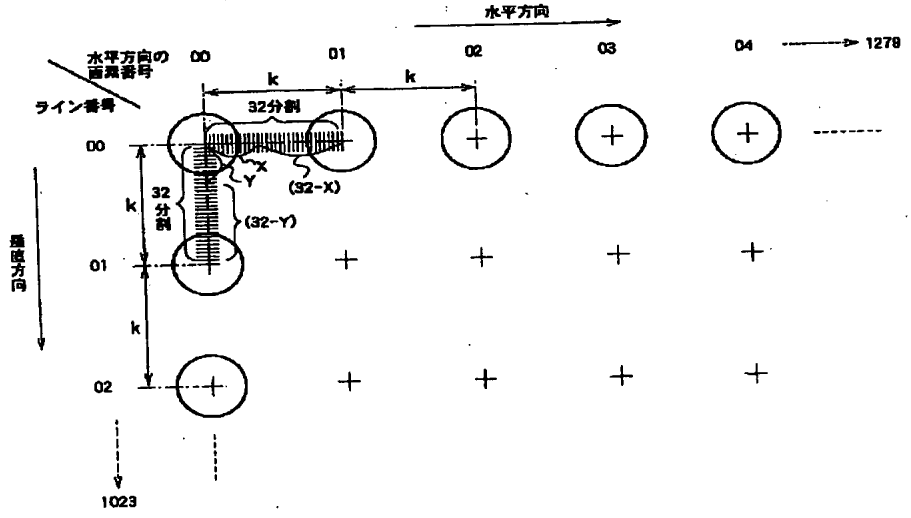
【図４】


プロジェクタを床上に設置した時の
台形歪み補正用画像を得るステップ
(a)
N
M
12 液晶パネル
原画像
(b)
大
垂直縮小倍率
小
12
垂直歪み補正
(c)
DLH
12
垂直歪み補正及び
水平歪み補正をした
台形歪み補正用画像
DLH
水平縮小倍率

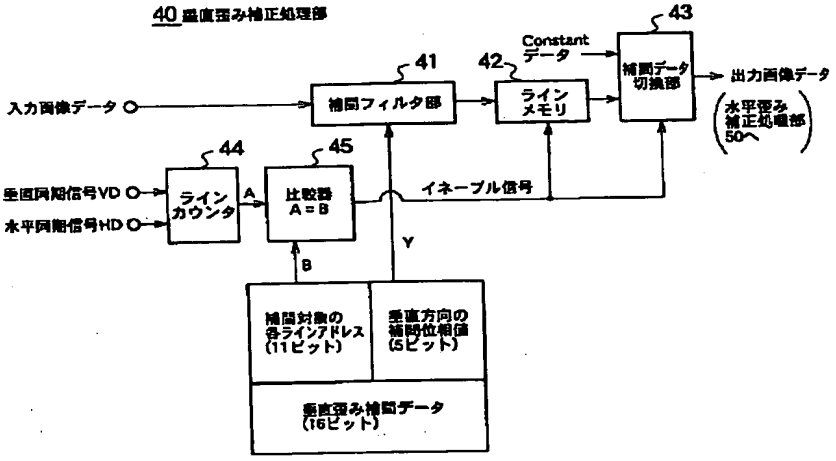
【図９】


画素番号
00
01
02
03
k
k
k
GK=32
GK=32
GK=32
入力ライン
出力ライン
-HS=-84
S=0
XF=28
HGK=58
00
-HS=-77
S=0
XF=31
HGK=54
01
-HS=-70
S=1
HGK=62
02
XF=2
03
04
05
06
07
08
09
10
11
12
H
各ラインでの補間開始

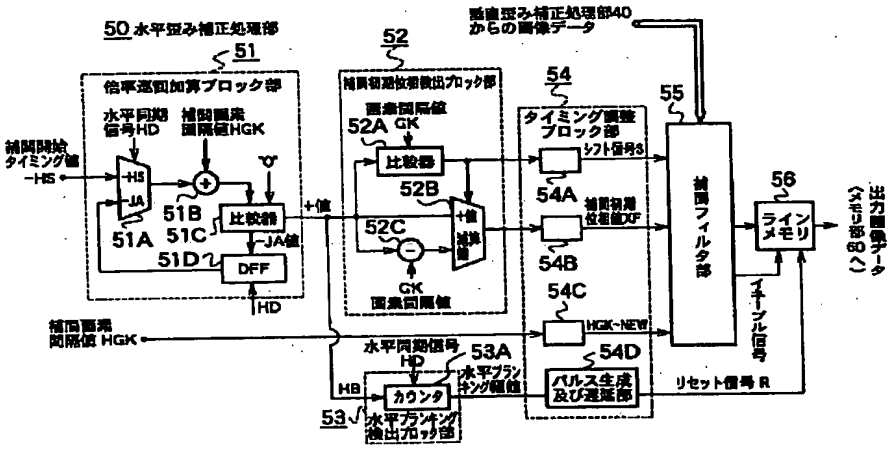
【図５】


水平方向
水平方向の
画素番号
ライン番号
00
01
02
03
04
1279
k
k
32分割
00
X
Y
(32-X)
32
分
割
k
(32-Y)
垂直方向
01
k
02
1023

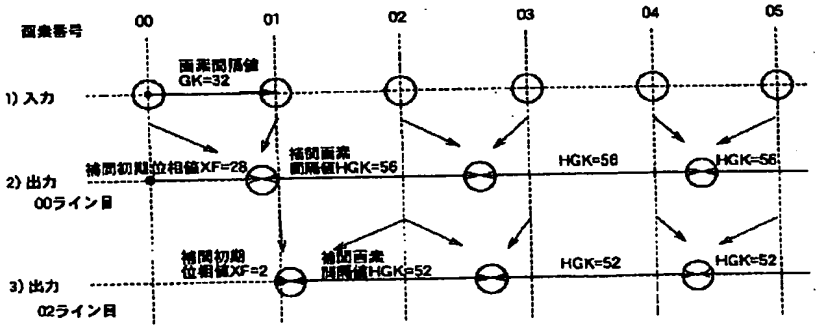
【図６】


40 垂直歪み補正処理部
43
Constant データ
41
42
補間データ切換部
出力画像データ
入力画像データ
補間フィルタ部
ラインメモリ
(水平歪み補正処理部50へ)
44
45
垂直同期信号VD
水平同期信号HD
ラインカウンタ
A
比較器 A=B
イネーブル信号
B
Y
補間対象の各ラインアドレス (11ビット)
垂直方向の補間位相値 (5ビット)
垂直歪み補間データ (16ビット)

【図８】


50 水平歪み補正処理部
垂直歪み補正処理部40からの画像データ
51
信号遅延加算ブロック部
52
補間初期位相値算出ブロック部
54
タイミング調整ブロック部
55
56
水平同期信号HD
補間画素間隔値HGK
補間開始タイミング値
画素間隔値
GK
比較器
シフト信号S
補間初期位相値XF
補間フィルタ部
ラインメモリ
出力画像データ (メモリ部60へ)
51A
51B
51C
51D
DFF
JA値
+値
減算器
52A
52B
52C
GK 画素間隔値
54A
54B
54C
54D
HGK-NEW
イネーブル信号
リセット信号 R
HD
HB
53A
水平ブランキング値
カウンタ
53
水平ブランキング検出ブロック部
パルス生成及び遅延部

【図１１】


画素番号
00
01
02
03
04
05
1) 入力
画素間隔値 GK=32
2) 出力 00ライン目
補間初期位相値XF=28
補間画素間隔値HGK=56
HGK=56
HGK=56
3) 出力 02ライン目
補間初期位相値XF=2
補間画素間隔値HGK=52
HGK=52
HGK=52

【図１０】

	メモリテーブル31に記憶した水平歪み補正データ					
ライン番号	画素間隔値 GK	補間開始タイミング値 -HS	補間画素間隔値 HGK	巡回回数 N	シフト信号 S	補間初期位相値 XF
00	32ステップ	-84ステップ	56ステップ	2	0	28ステップ
01	32ステップ	-77ステップ	54ステップ	2	0	31ステップ
02	32ステップ	-70ステップ	52ステップ	2	1	2ステップ
03	32ステップ	-63ステップ	50ステップ	2	1	5ステップ
04	32ステップ	-56ステップ	48ステップ	2	1	8ステップ
05	32ステップ	-49ステップ	46ステップ	2	1	11ステップ
06	32ステップ	-42ステップ	44ステップ	1	0	2ステップ
07	32ステップ	-35ステップ	42ステップ	1	0	7ステップ
08	32ステップ	-28ステップ	40ステップ	1	0	12ステップ
09	32ステップ	-21ステップ	38ステップ	1	0	17ステップ
10	32ステップ	-14ステップ	36ステップ	1	0	22ステップ
11	32ステップ	-7ステップ	34ステップ	1	0	27ステップ
12	32ステップ	0ステップ	32ステップ	0	0	0ステップ

フロントページの続き

(51)Int.Cl.[7]		識別記号	FI		テーマコード（参考）
Ｇ０９Ｇ	3/20	６２３	Ｇ０９Ｇ	3/20	６２３Ｍ
		６３１			６３１Ｒ
		６３２			６３２Ｂ
					６３２Ｃ
		６８０			６８０Ｃ
Ｈ０４Ｎ	5/74		Ｈ０４Ｎ	5/74	Ｄ

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JJ06